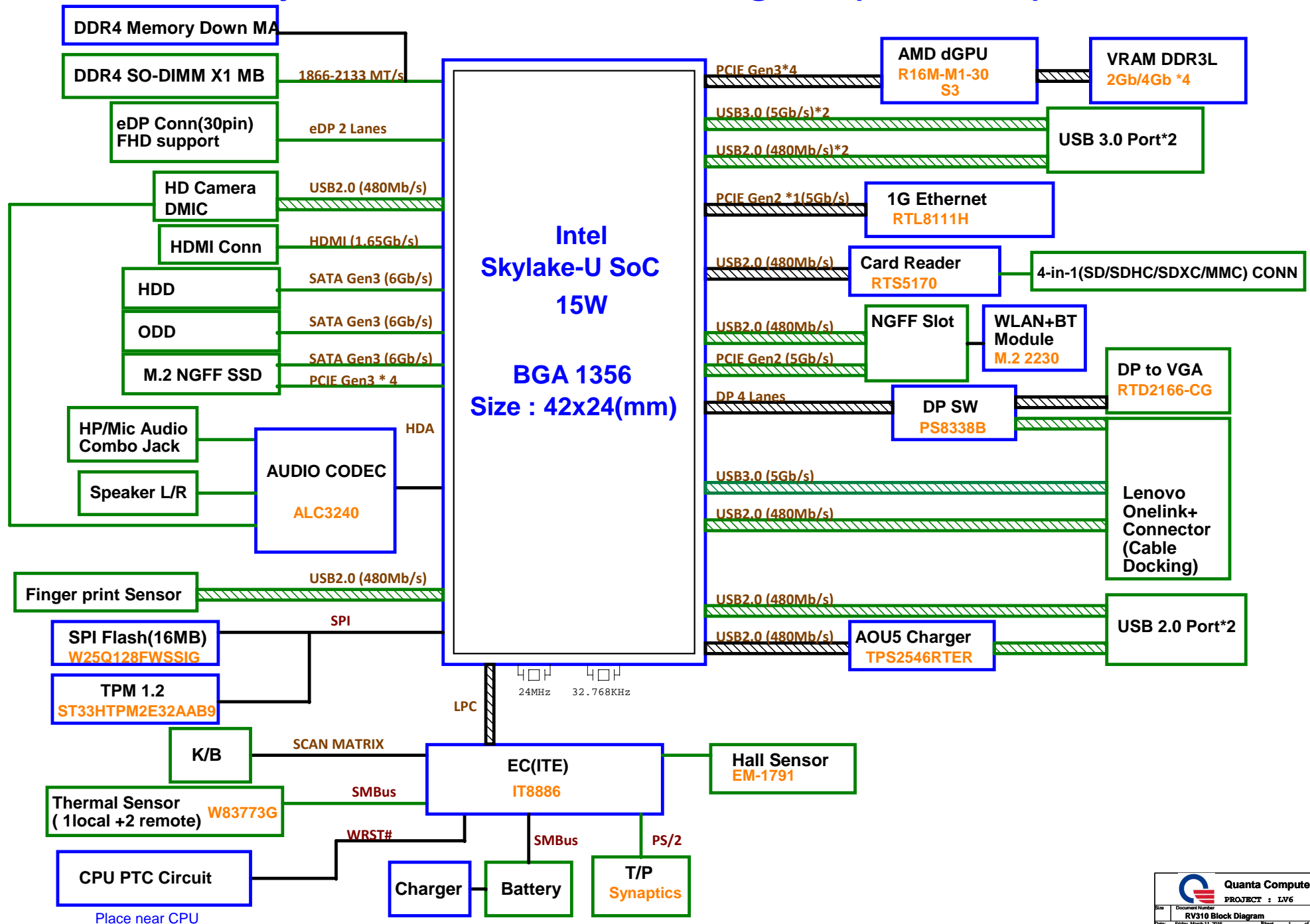
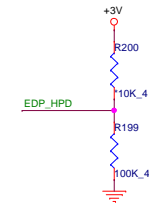


Intel Skylake-U Platform Block Diagram (Windows)

01

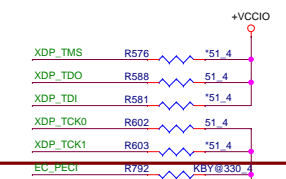




H_PROCHOT# R590 1K 4 +VCCSTPLL

PM_THRMTRIP#_R R583 1K 4 +VCCSTPLL

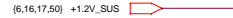
B2A



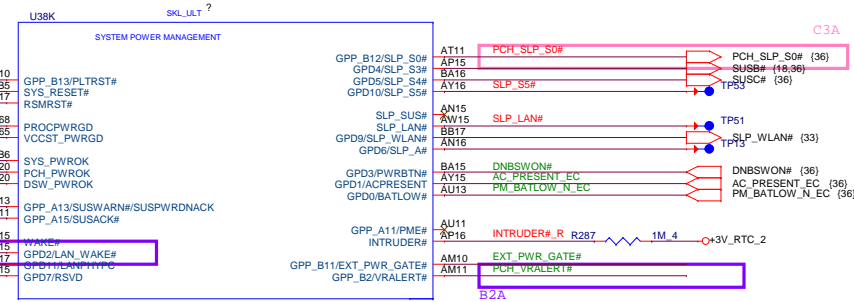
PLACE NEAR CPU



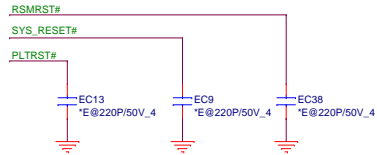
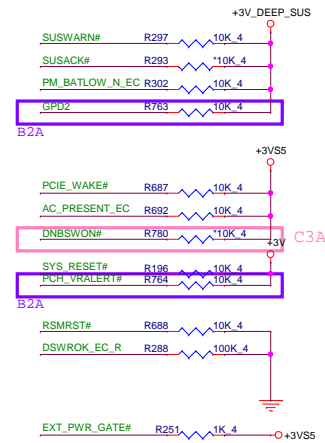
03



(10,11,14,15,17) +3V_DEEP_SUS
(2,10,11,12,13,14,15,17,18,25,26,27,29,30,31,34,36,37,38,40,41,42,45,49,52,53,54) +3V5
(34,35,38,39,41,42,44,45,48,50,51,53,54,56) +5V55
(2,6,53,56) +VCCIO
(2,5,6,9,45,53,56) +VCCSTPLL
(13,15) +3V_RTC_2



PCH Pull-high/low(CLG)

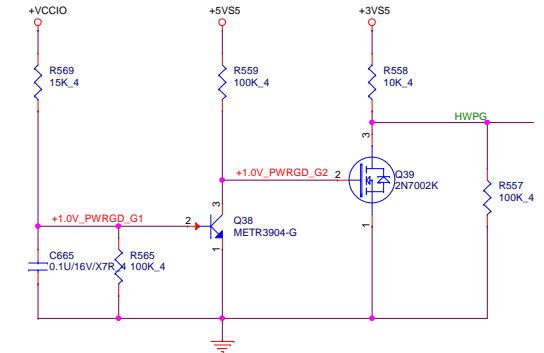
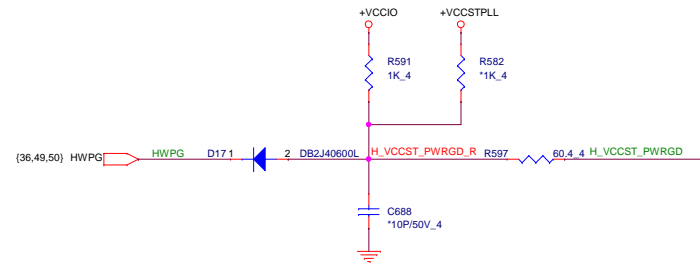
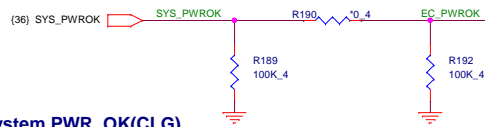



RSMRST# R285 0.4 S DSWROK_EC_R

PLTRST#(CLG)

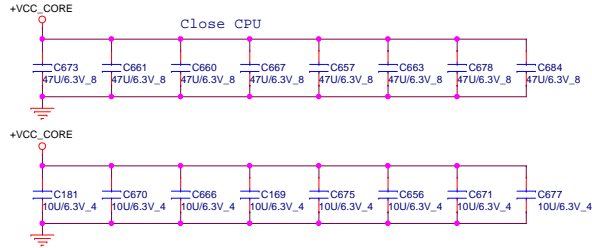
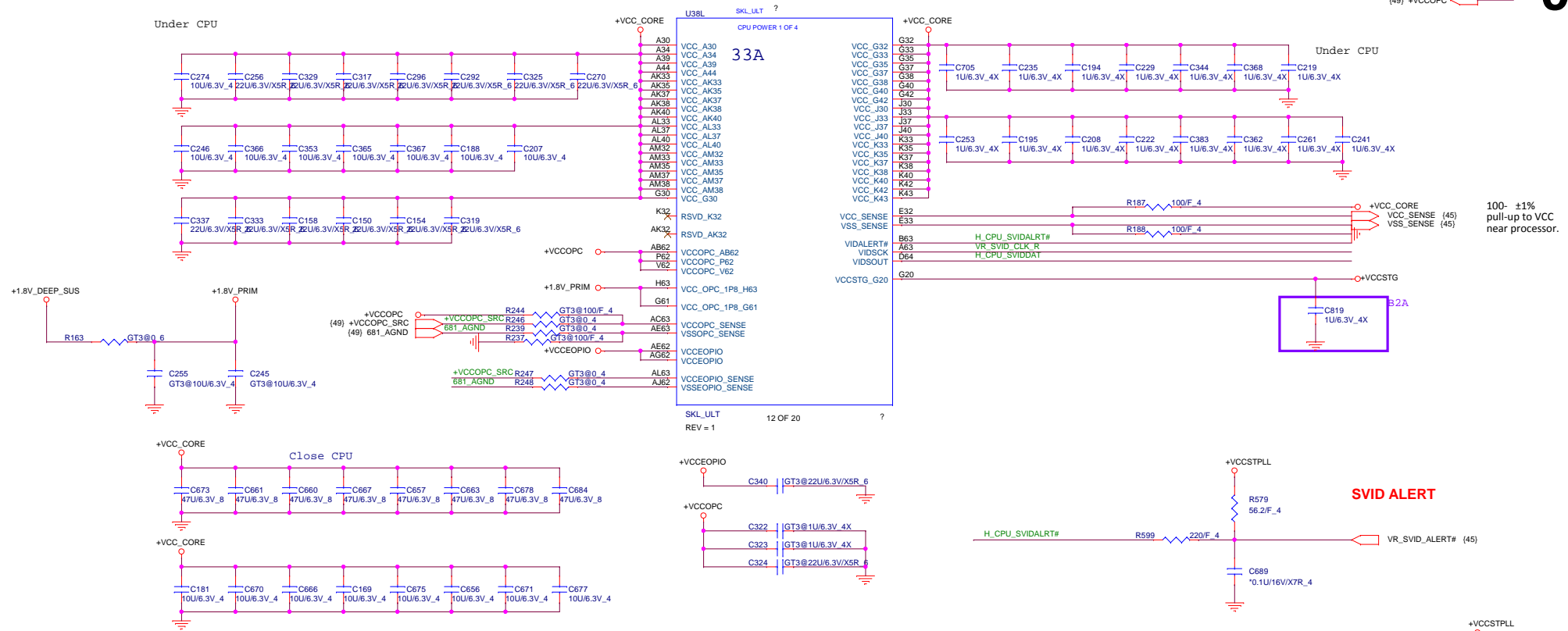


System PWR_OK(CLG)

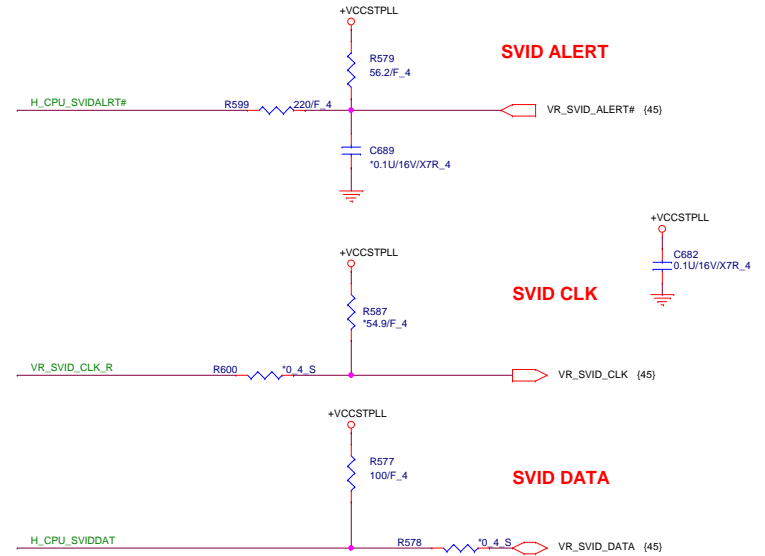


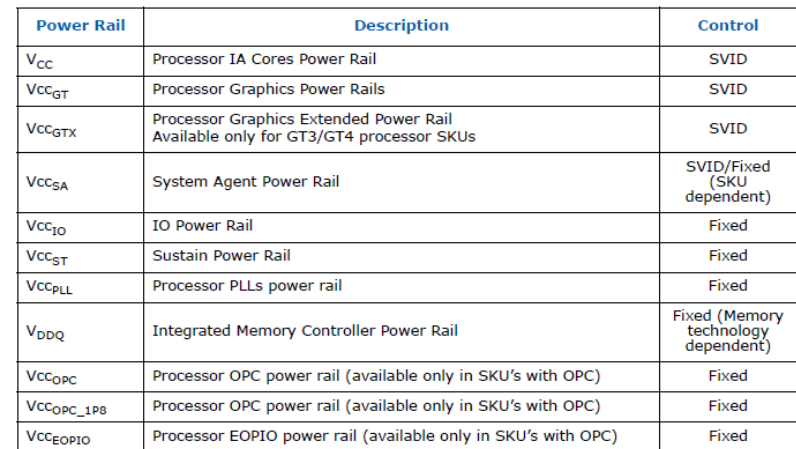
 Quanta Computer Inc. PROJECT : LV6		
Size	Document Number	Rev 1A
SKYLAKE 3/15(PowerManger)		
Date: Friday, March 11, 2016	Sheet 4 of 61	

Under CPU

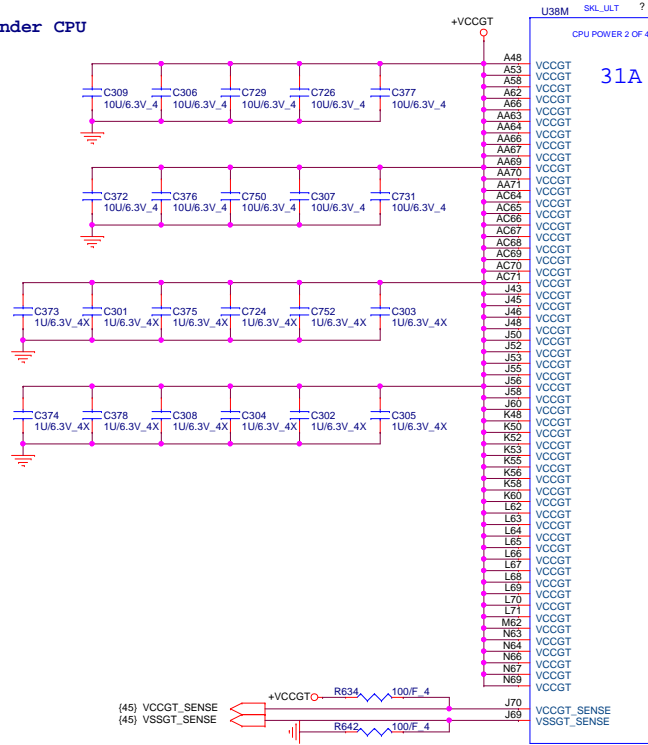


Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTx}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

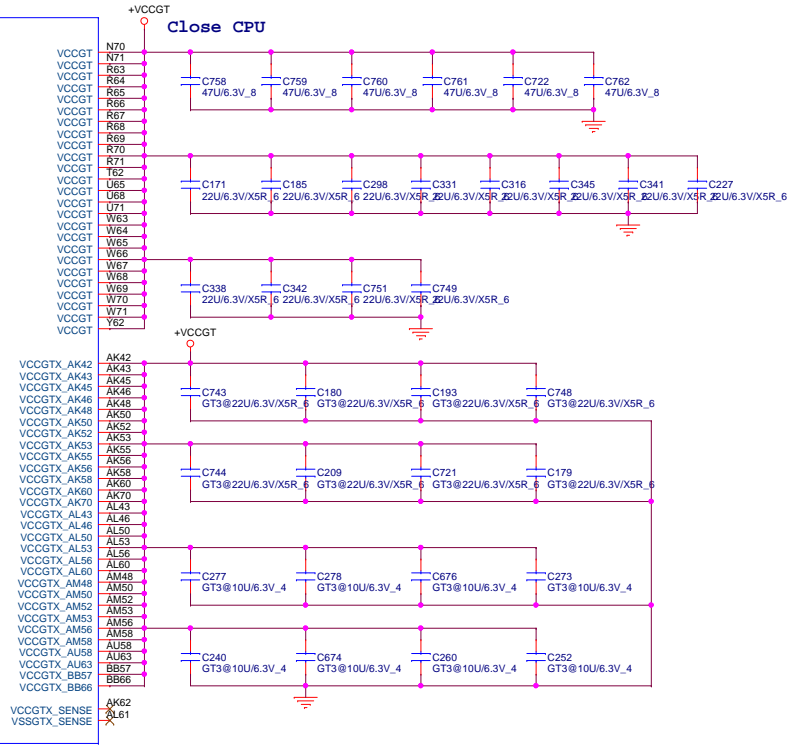




Under CPU



Close CPU

SKL_ULT 13 OF 20
REV = 1

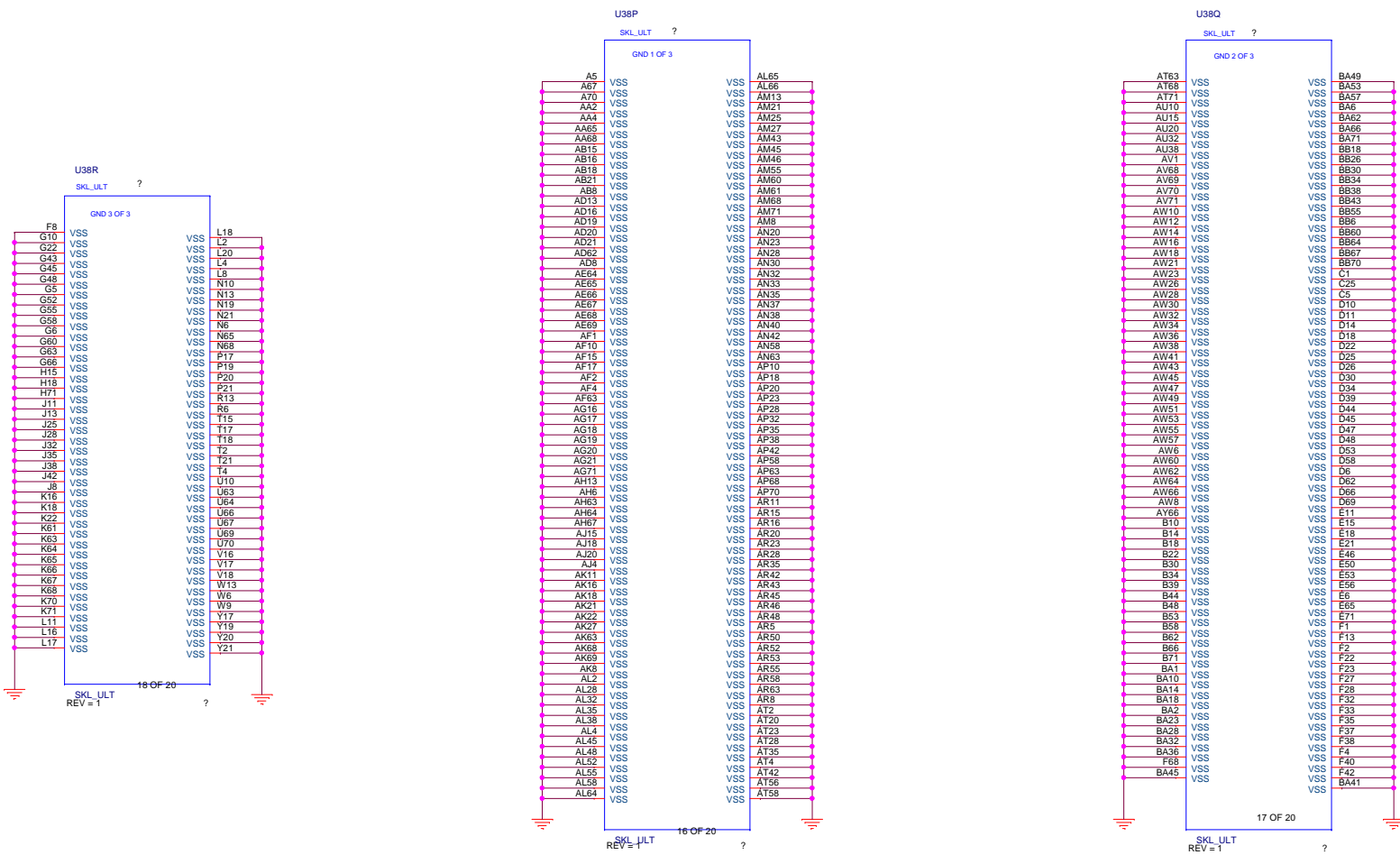
Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1PB}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

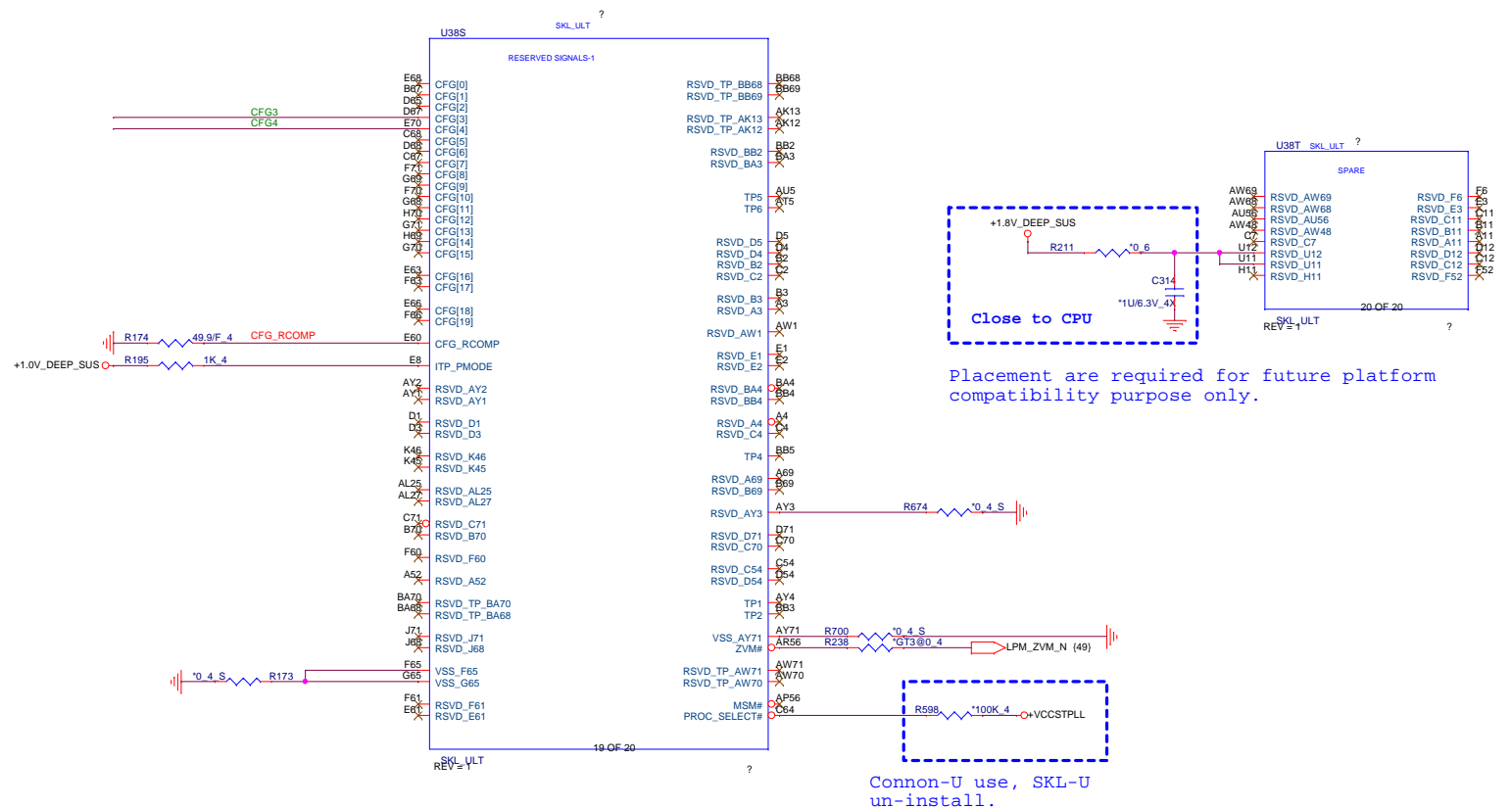


Quanta Computer Inc.

PROJECT : LV6

Size	Document Number	Rev
	SKYLAKE 6/15 (POWER-3)	1A
Date:	Friday, March 11, 2016	Sheet 7 of 61

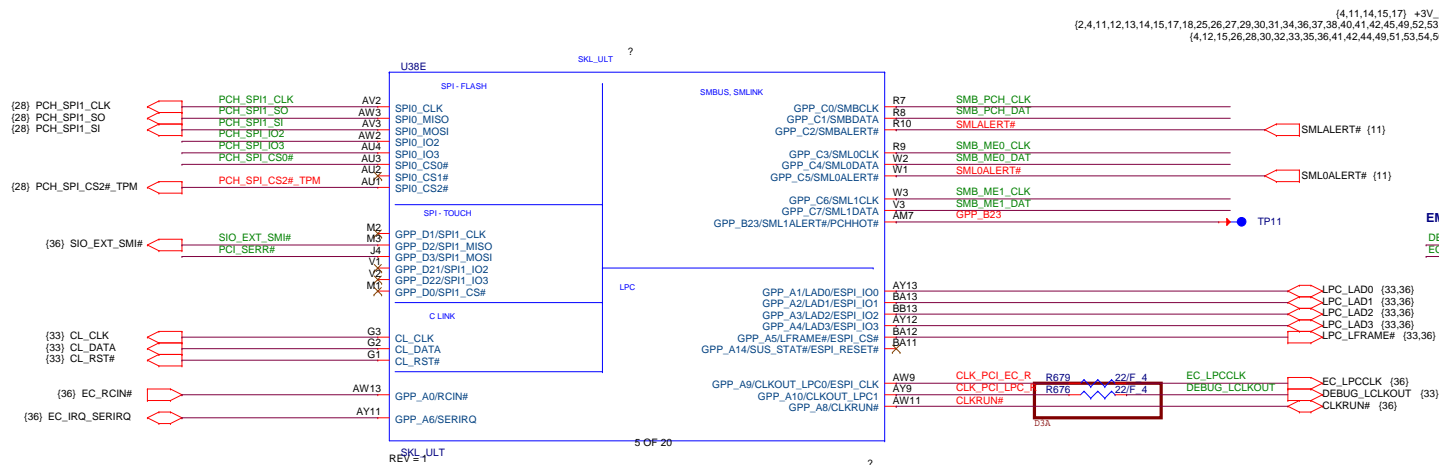




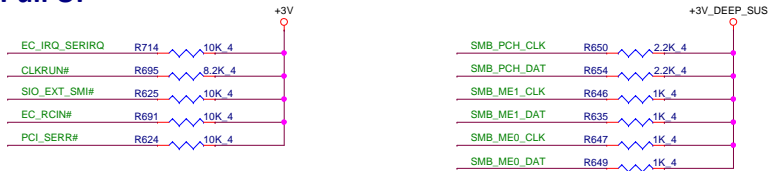
Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R611 1K 4
CFG4 (DP Presence Strap)	Disable: No physical DP attached to eDP	Enable: An ext DP device is connected to eDP	CFG4 R617 1K 4



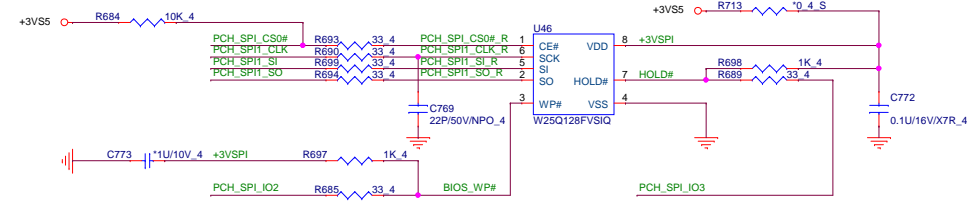
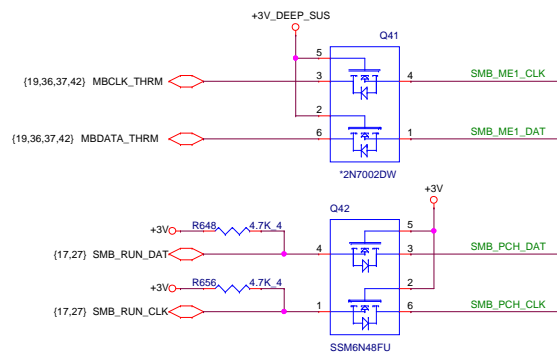
GPIO Pull UP



PCH SPI ROM(CLG)



SMBus/Pull-up(CLG)



Vender	Size	P/N
EON	16MB	AKE3DZLNKQ00(EN25QH128AHIP)
GGD	16MB	AKE3DF00Q00 (GD25B128CSIGR)
Socket		DFHS08FS023

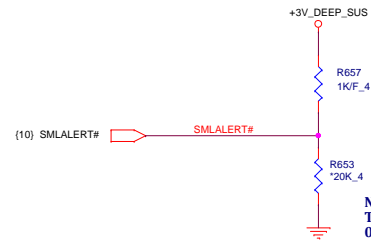
Quanta Computer Inc. PROJECT : LV6		
Size	Document Number	Rev 1A
	SKYLAKE 9/15(SPI/LPC/SM)	
Date:	Friday, March 11, 2016	Sheet 10 of 61

Functional Strap Definitions

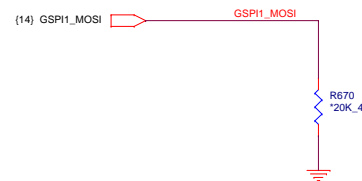
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



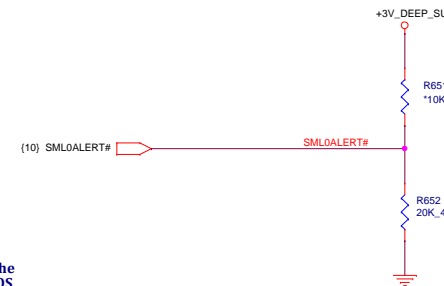
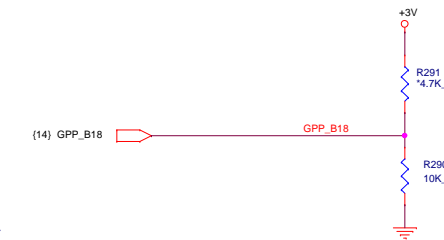
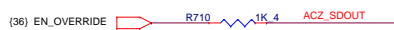
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



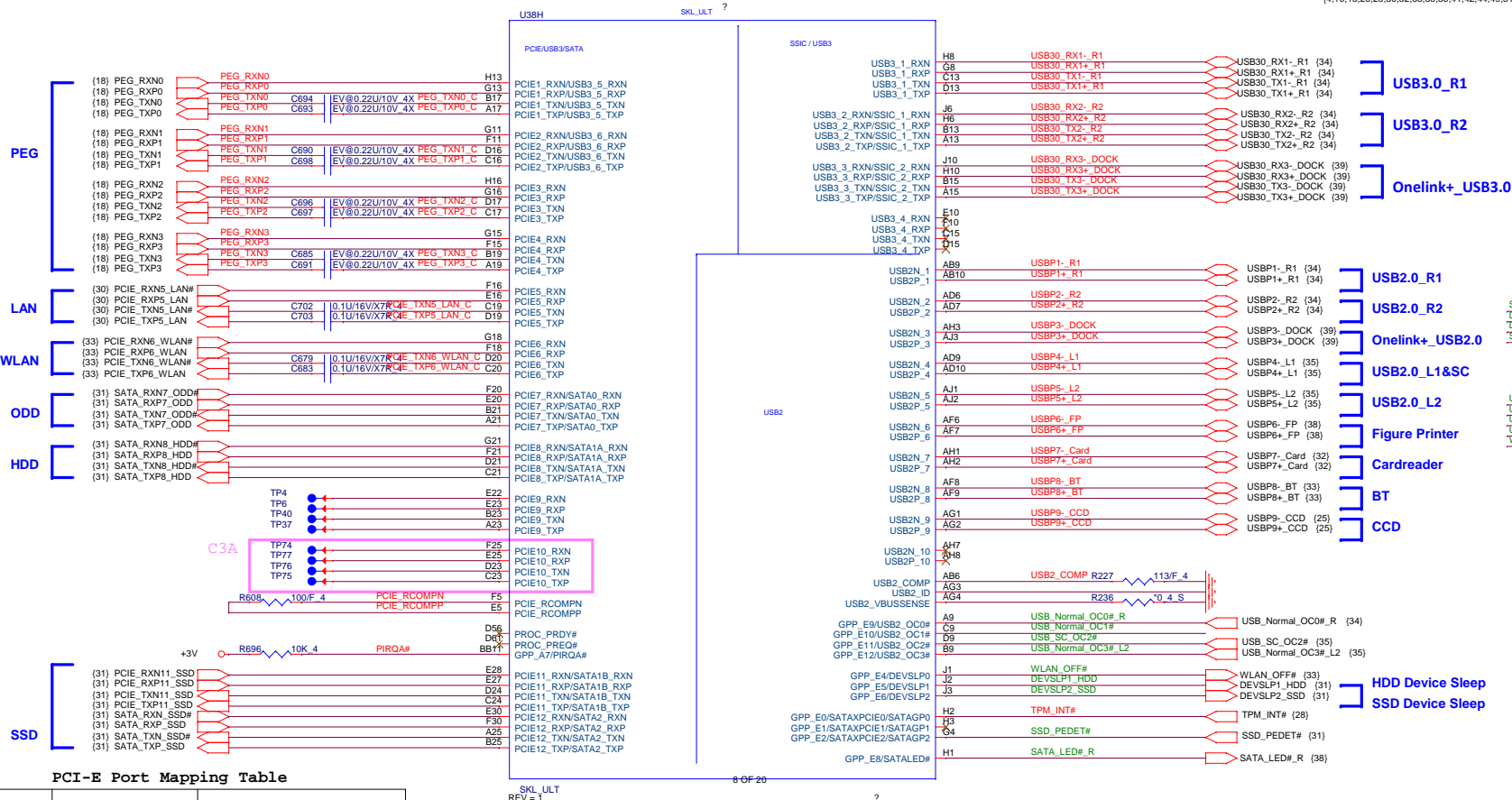
No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.
Bit 10 Boot BIOS Destination
0 SPI
1 LPC



No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.

No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

No Boot:
The signal has a weak internal pull-down.
0 = LPC is selected for EC.
1 = eSPI is selected for EC.



PCI-E Port Mapping Table

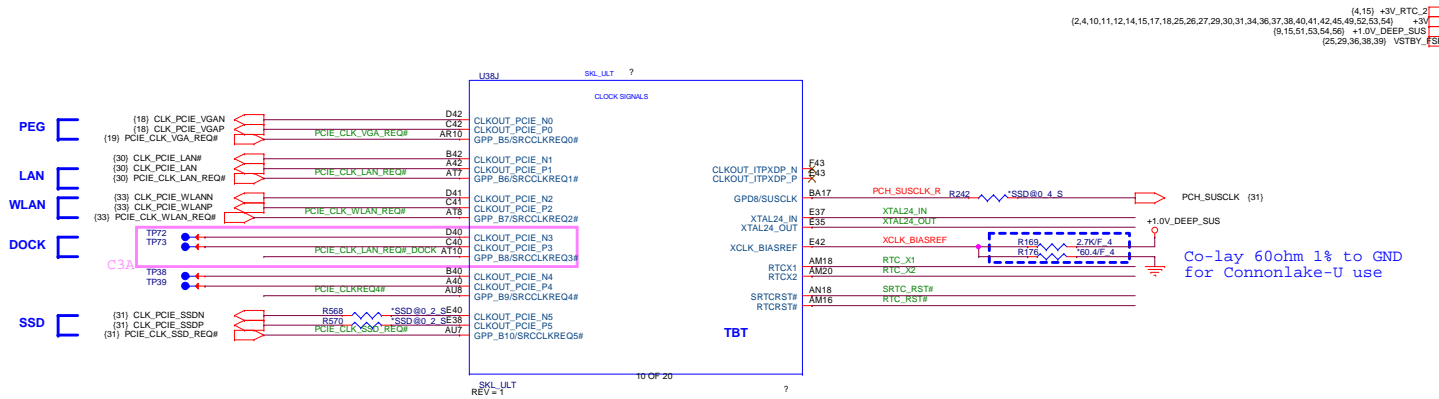
PCI-E Port	Function	CLK RQ Port	Function
Port1		Port0	dGPU
Port2		Port1	LAN
Port3	dGPU	Port2	WLAN
Port4		Port3	DOCK
Port5	LAN	Port4	Un-used
Port6	WLAN	Port5	SSD
Port7	ODD		
Port8	HDD		
Port9	Un-used		
Port10	DOCK		
Port11	SSD		
Port12	if PCIe Bus will lane reverse. if SATA BUS is SATA2.		

USB3.0 Port Mapping Table

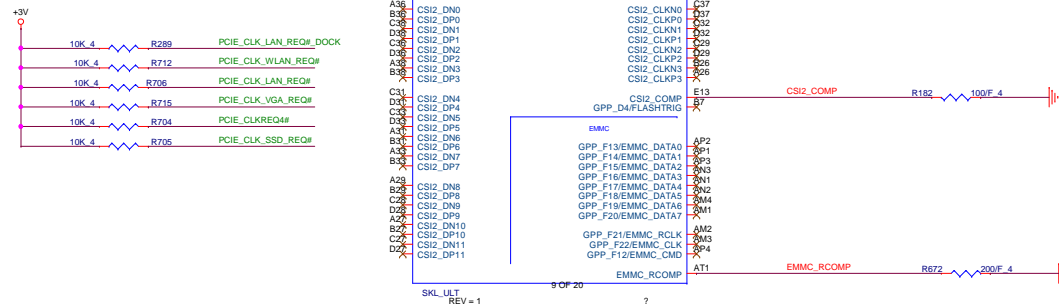
USB3.0	Function
PORT-1	USB3.0_R1
PORT-2	USB3.0_R2
PORT-3	USB3.0_DOCK
PORT-4	

USB2.0 Port Mapping Table

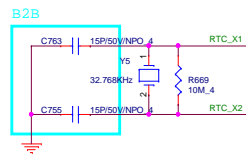
USB2.0	Function
PORT-1	USB2.0_R1
PORT-2	USB2.0_R2
PORT-3	USB2.0_DOCK
PORT-4	USB2.0_L1_S&C
PORT-5	USB2.0_L2
PORT-6	Figure Printer
PORT-7	Cardreader
PORT-8	BT
PORT-9	CCD
PORT-10	NC



CLK_REQ/Strap Pin(CLG)

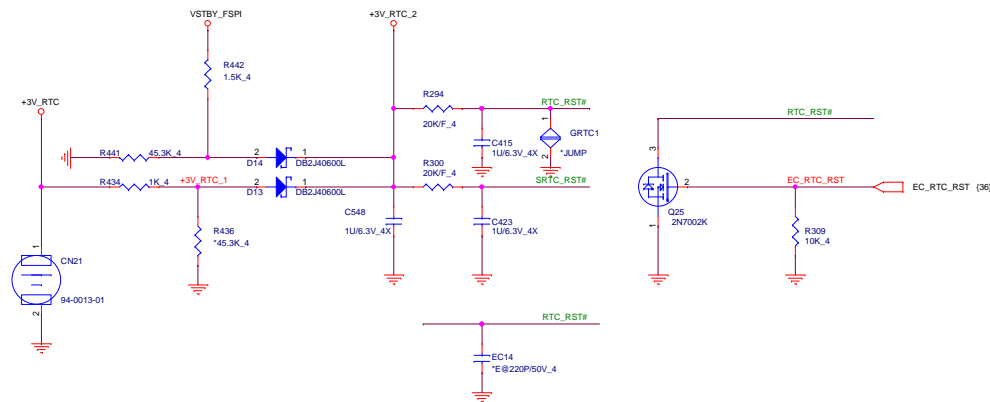


RTC Clock 32.768KHz (RTC)<RTC>

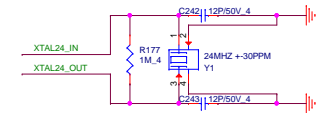


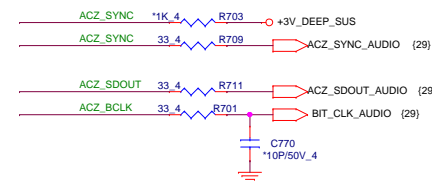
RTC Circuitry (RTC)<RTC>

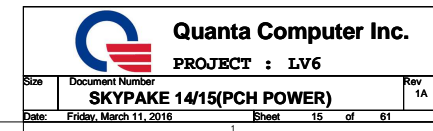
RTC Power trace width 20mils.

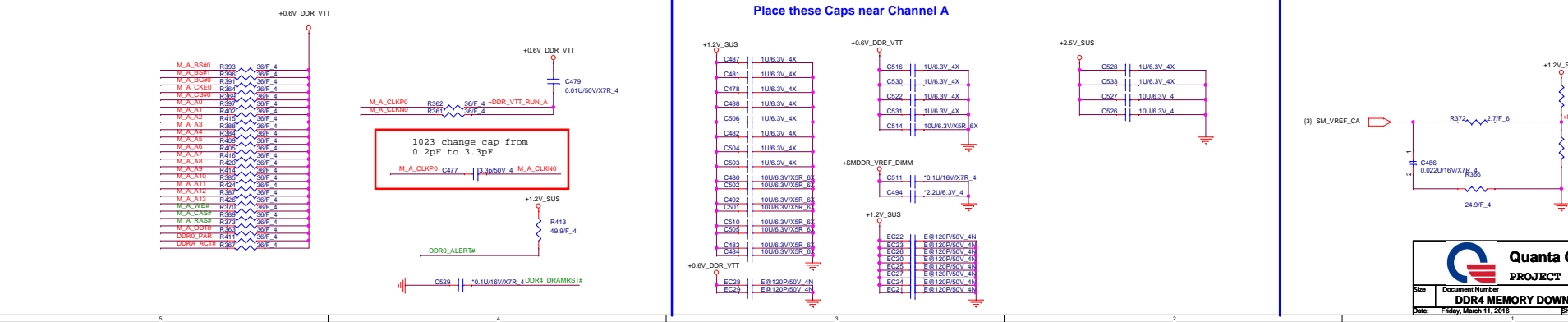
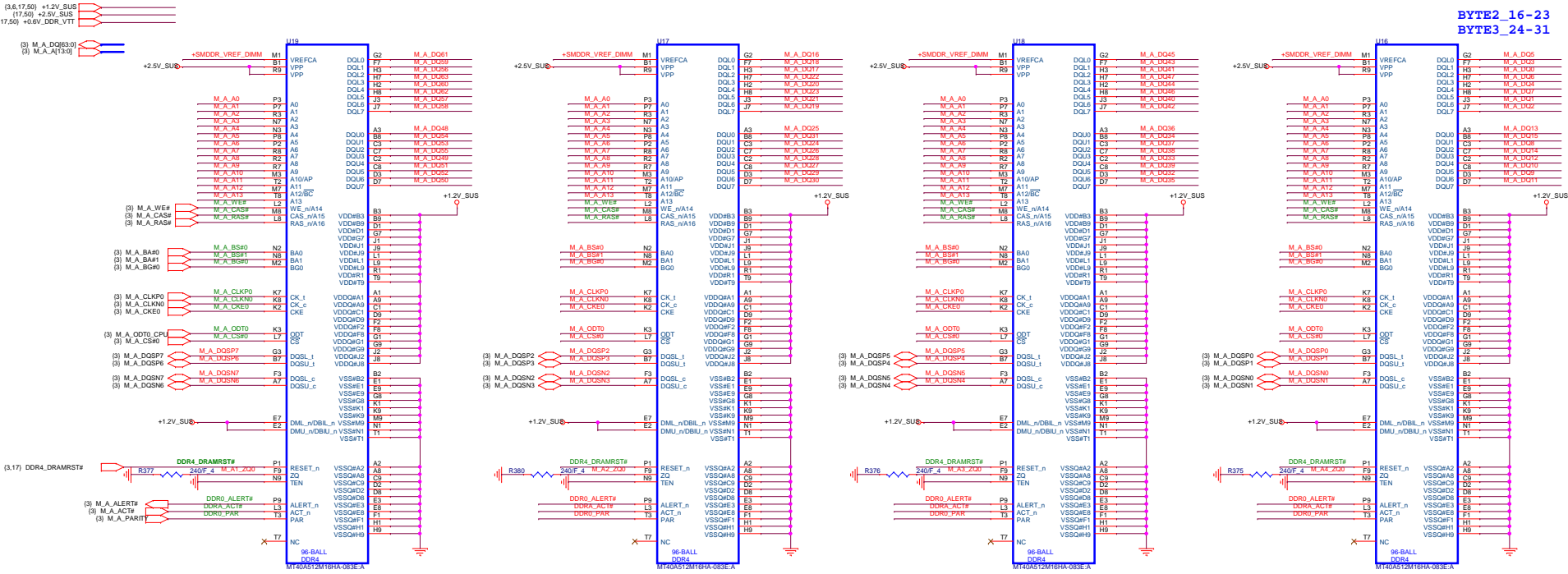


External Crystal and Green Clock



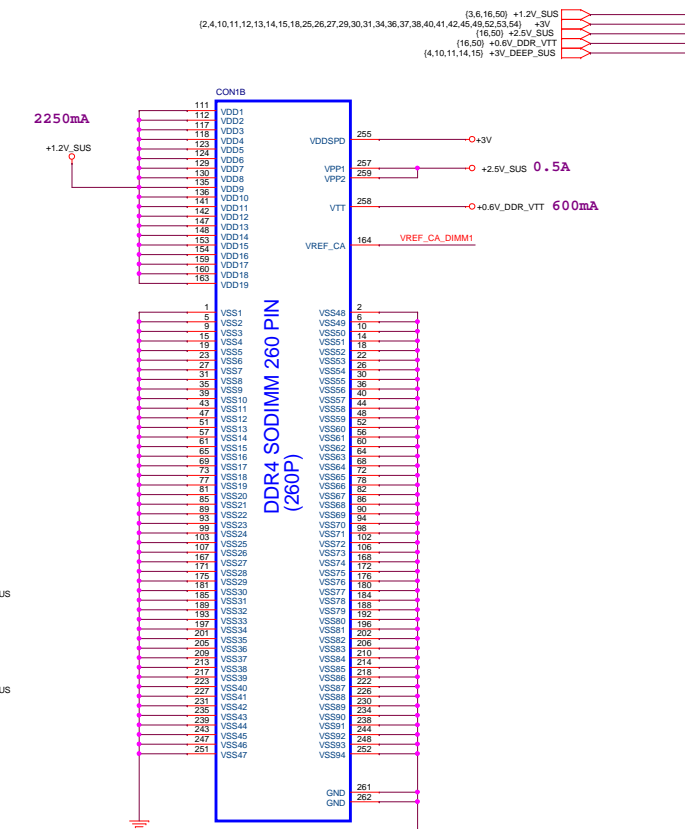
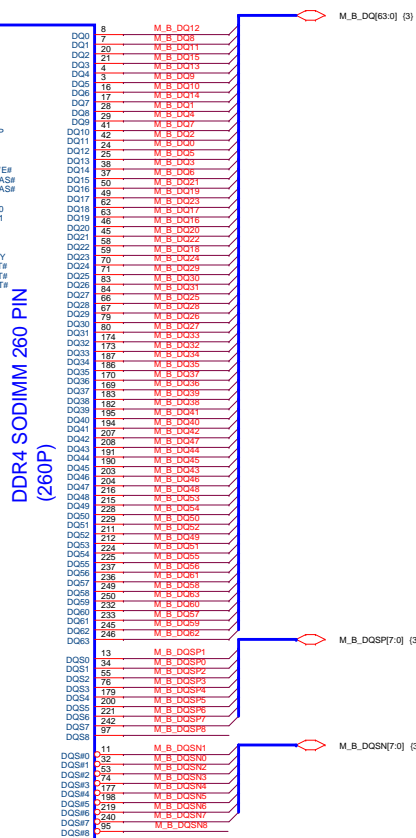
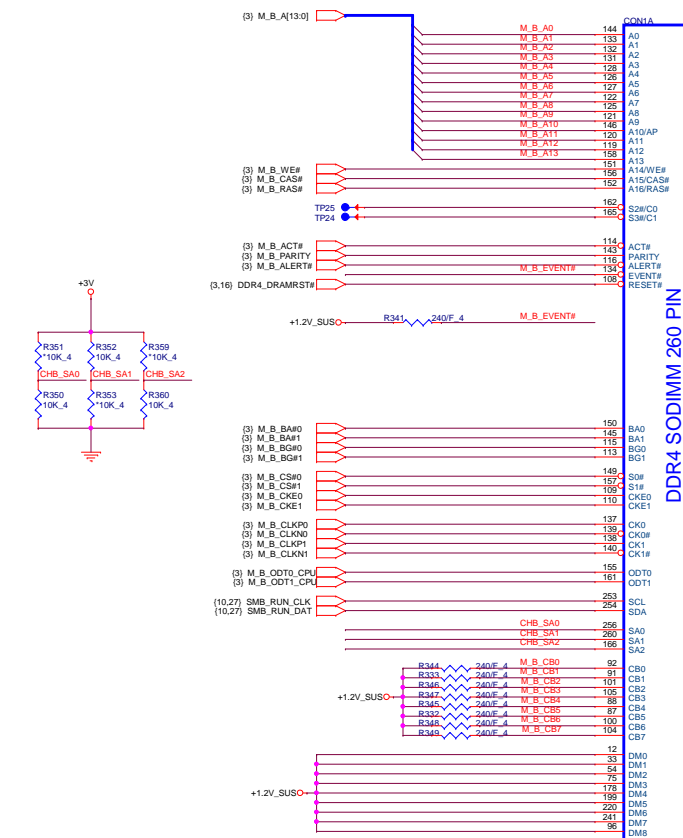




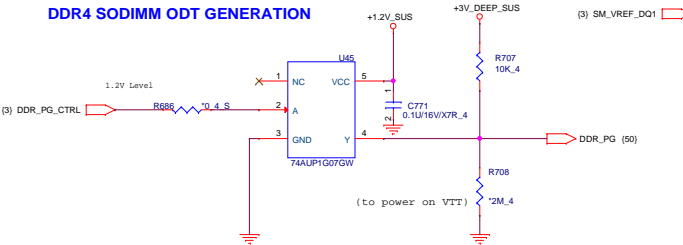


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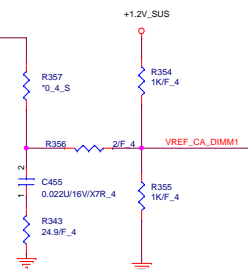
Size	Document Number	Rev
	DDR4 MEMORY DOWN	1A
Date	Friday, March 11, 2016	Sheet 16 of 61



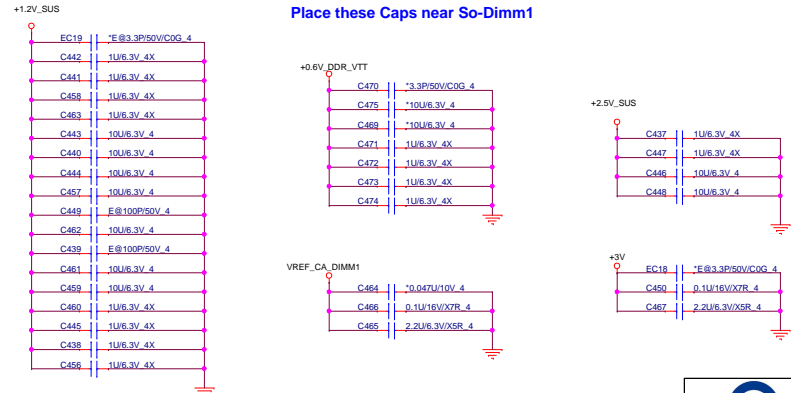
DDR4 SODIMM ODT GENERATION

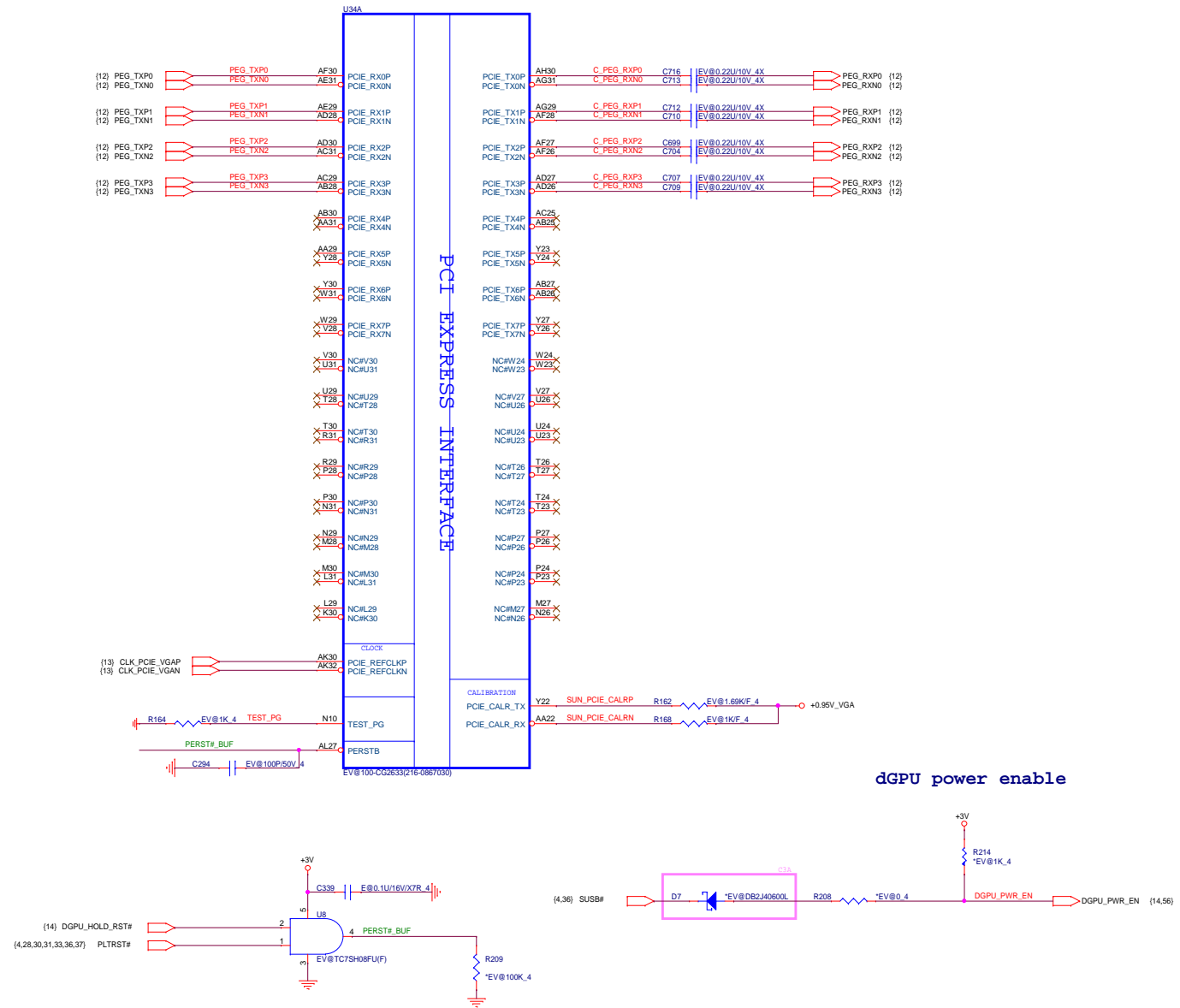


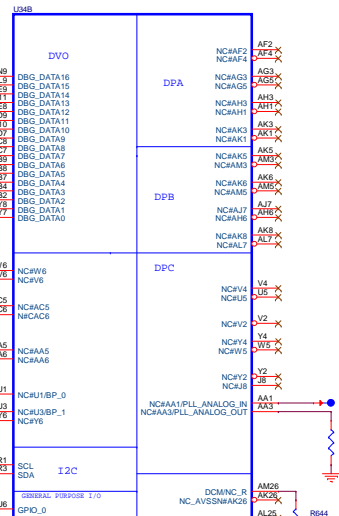
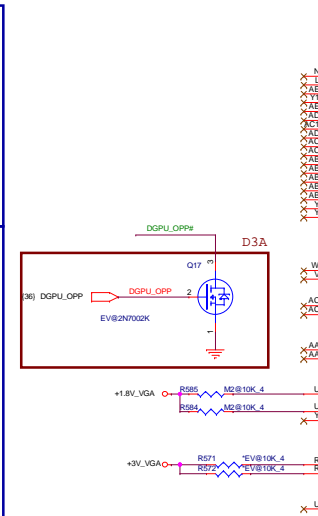
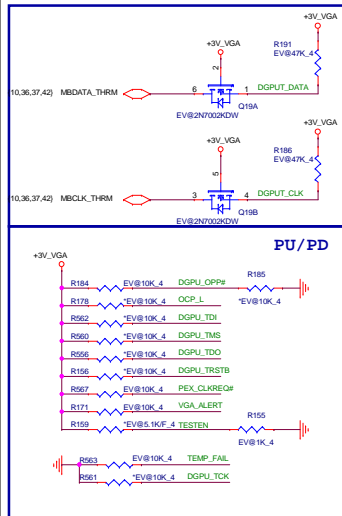
VREF CA DIMM1 Solution



Place these Caps near So-Dimm1





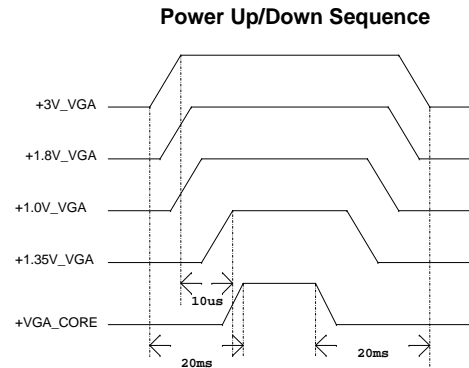


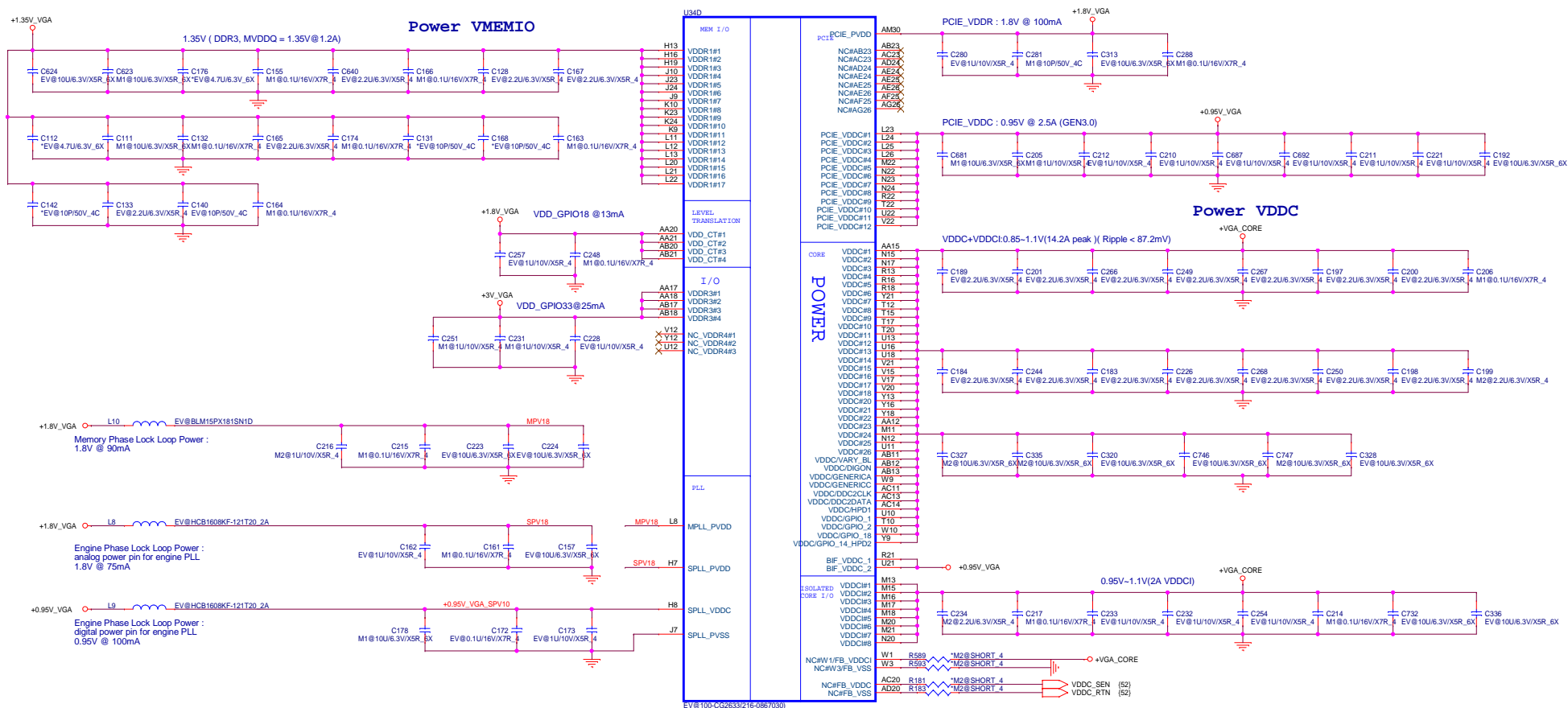


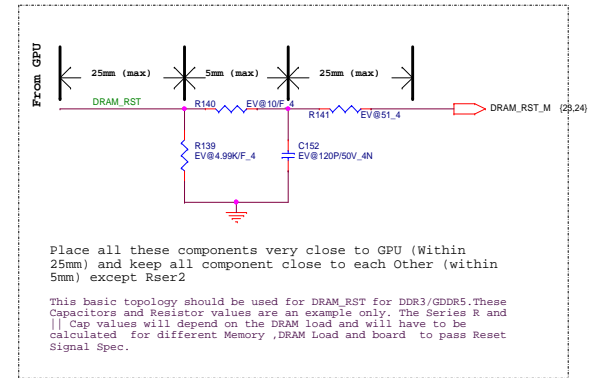
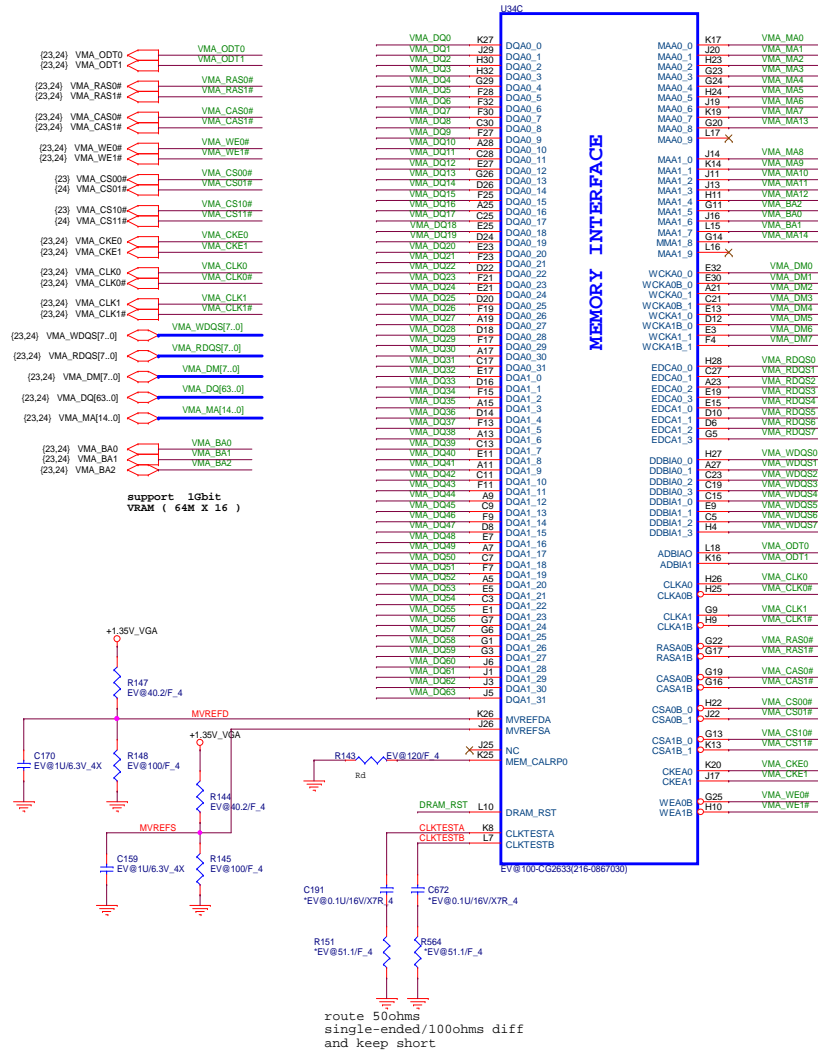
All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ μ s.

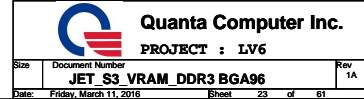
It is recommended that the 3.3-V rail ramp up first. The 3.3-V, 1.8-V, and 1.0-V rails must reach their ready state at least 10 μ s before VDDC, VDDCI, and VMEMIO start to ramp up.

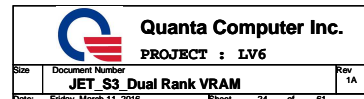
For power down, reversing the ramp-up sequence is recommended.

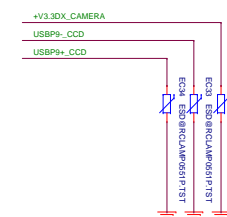
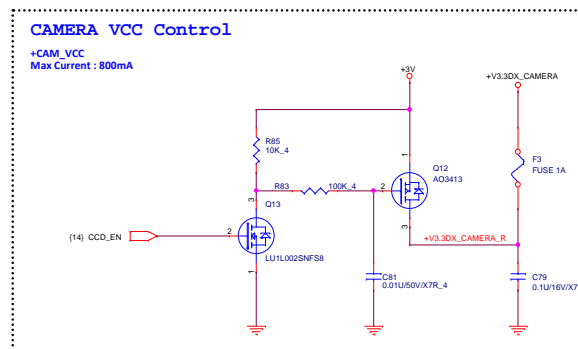
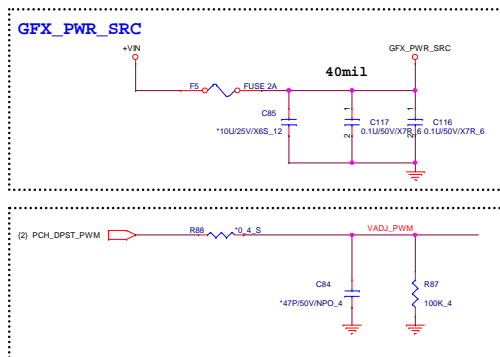
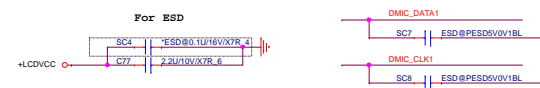
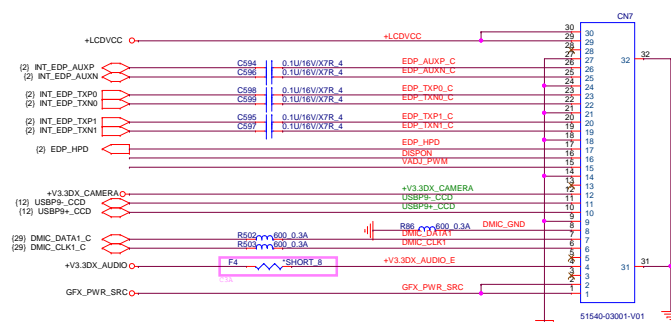
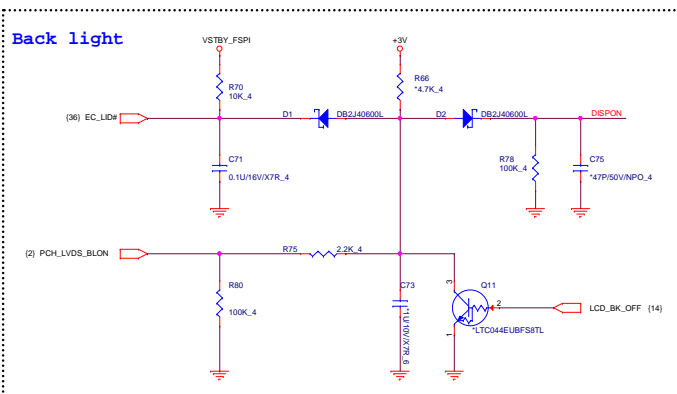
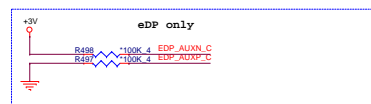
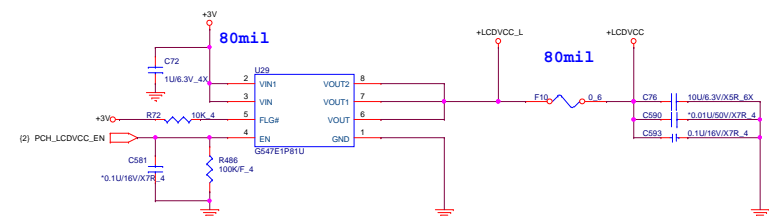




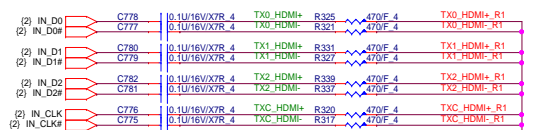




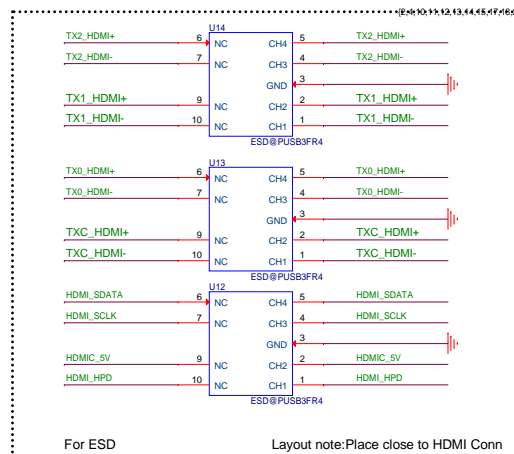
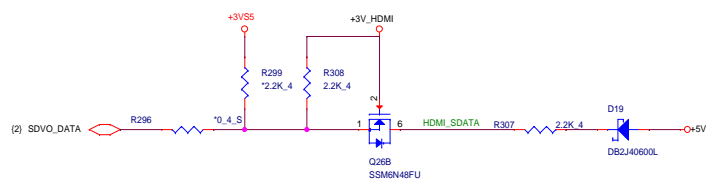
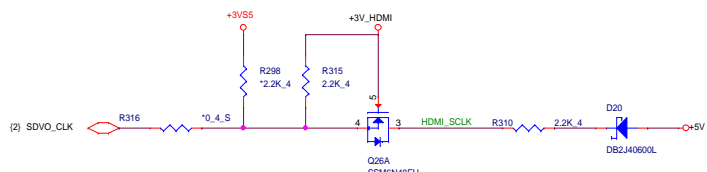
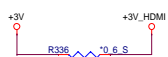
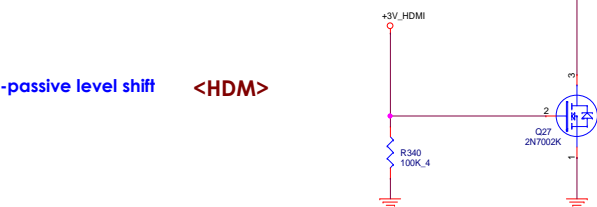




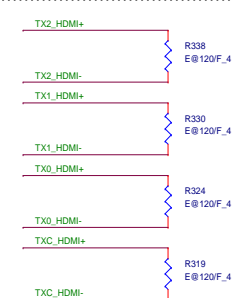
HDMI Conn <HDM>



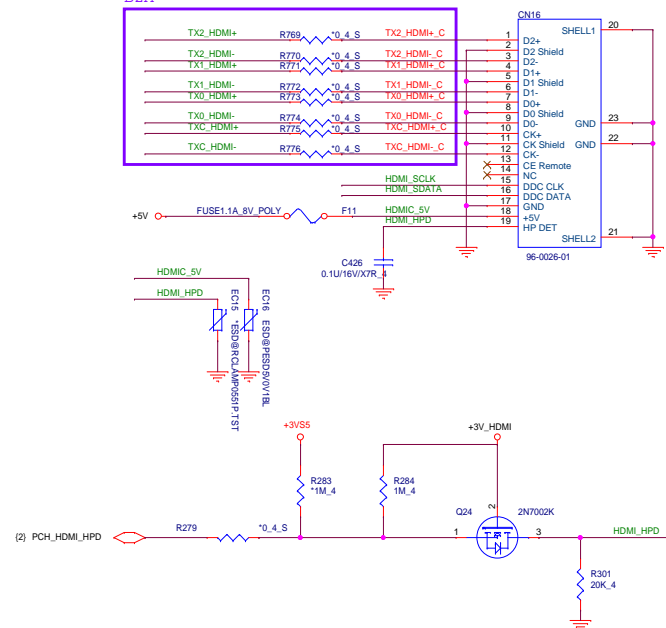
HDMI-passive level shift <HDM>

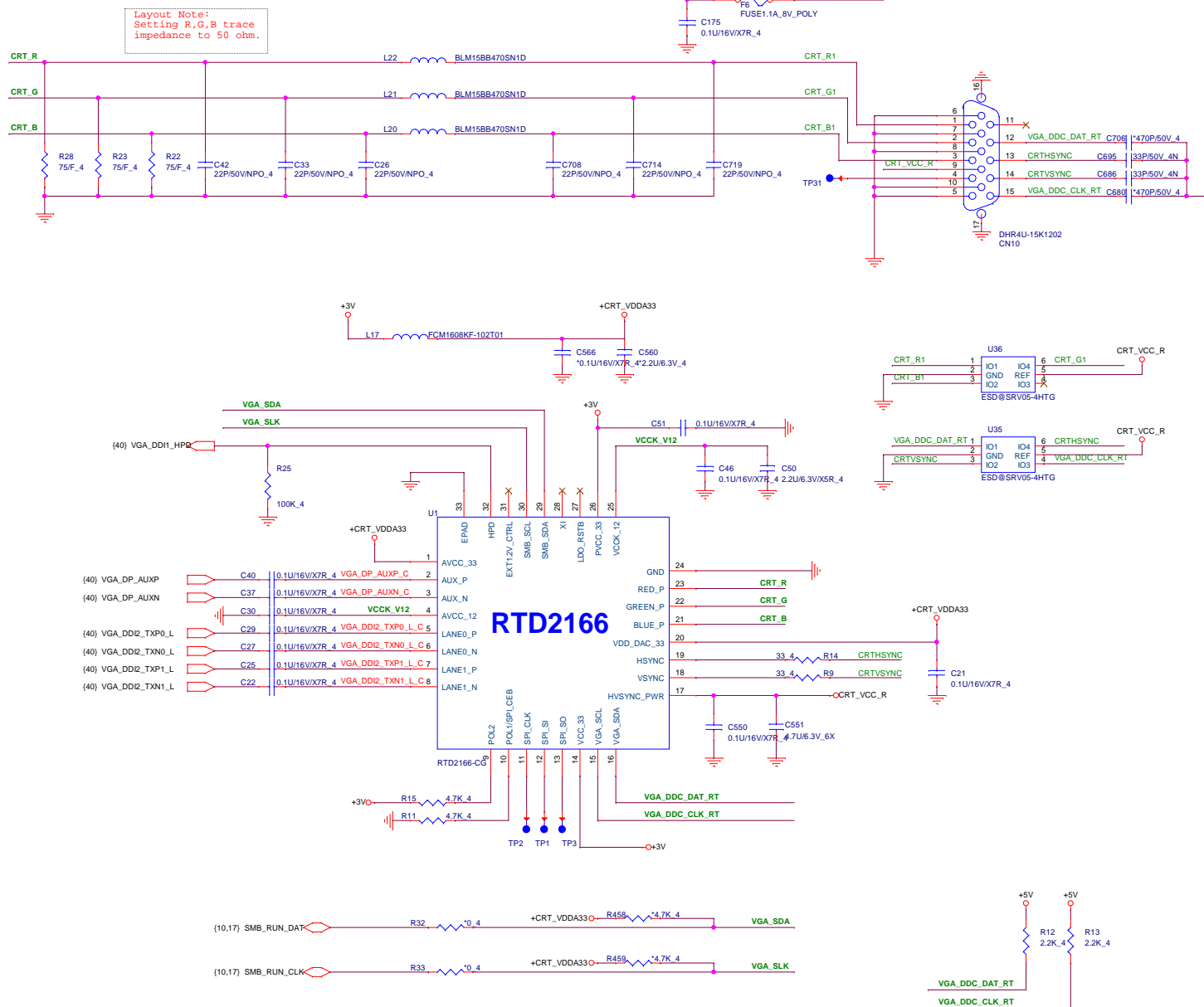


EMI reserve for HDMI



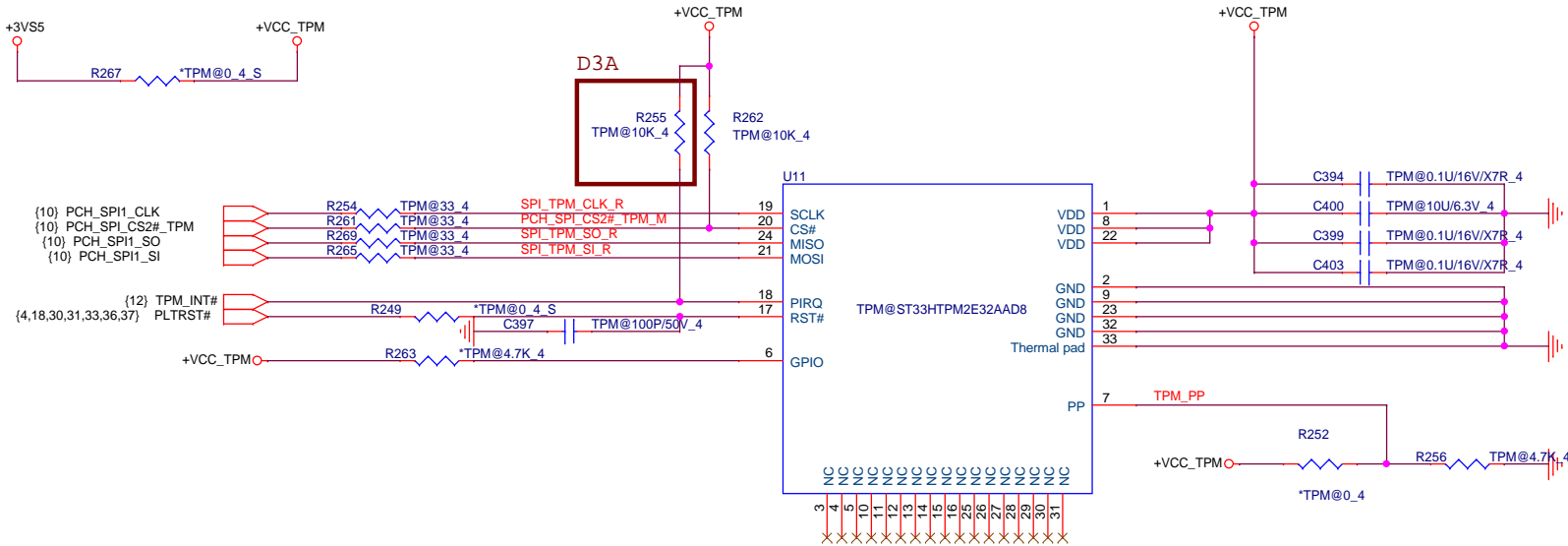
B2A





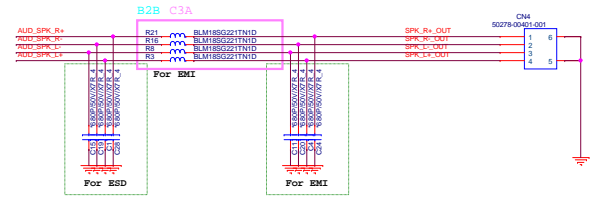
(2,4,10,11,12,13,14,15,17,18,25,26,27,29,30,31,34,36,37,38,40,41,42,45,49,52,53,54)
(4,10,12,15,26,30,32,33,35,36,41,42,44,49,51,53,54,56)

+3V
+3VS5

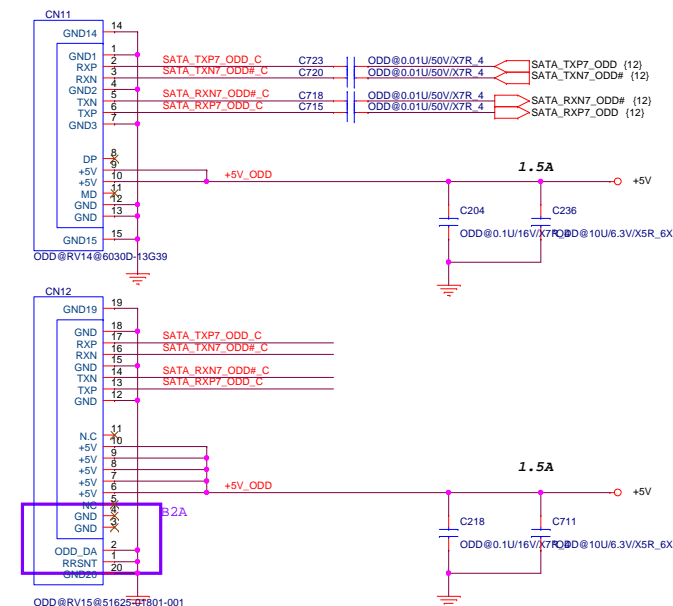


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SATA ODD <ODD>



The diagram illustrates the internal circuitry of an NGFF Key M SSD, specifically the NASMO-S6701-TSH4 model. It shows the connection of various signals to the CN13 connector. Key components include the NAND flash (S6701-TSH4), a controller (Q18), and several support components like resistors (R225, R643, R615, R243, R241, C385) and capacitors (C742, C741, C739, C738, C736, C735). The diagram details the connection of SATA signals (RXN, RXP, TXN, TXP) and PCIe signals (RXN1, RXP1, TXN1, TXP1) to the SSD pins. Power and ground connections for V3Vaux and GND are also shown. The diagram is labeled 'NGFF - Key M' and 'SSD@NASMO-S6701-TSH4'.

60 mil 1.5A

+3V

R231

*SSD@0.8 S

+V3DX_HDD

C357

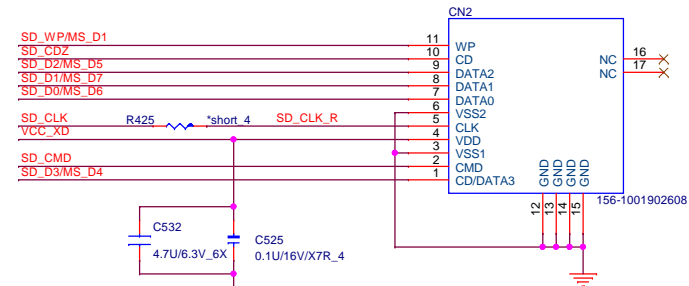
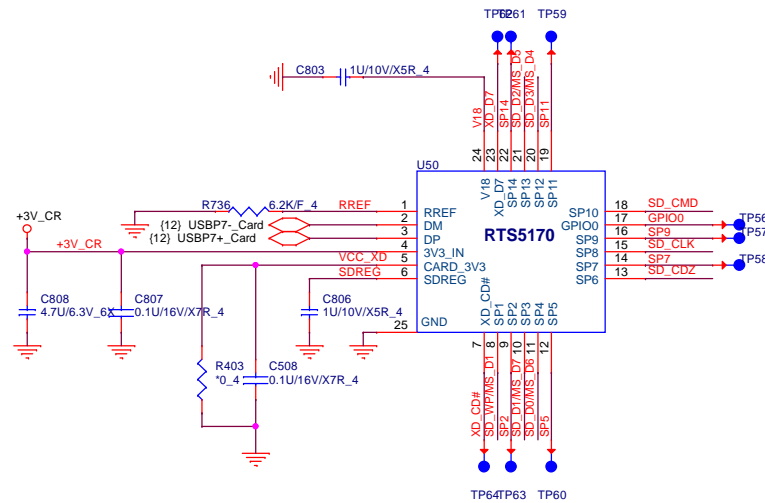
C384

C356

SSD@10U/6.3V/X5R_6X

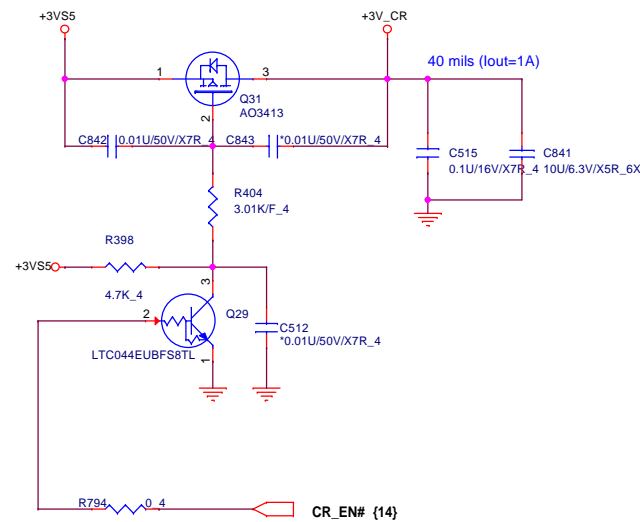
SSD@10U/16V/X7R_4

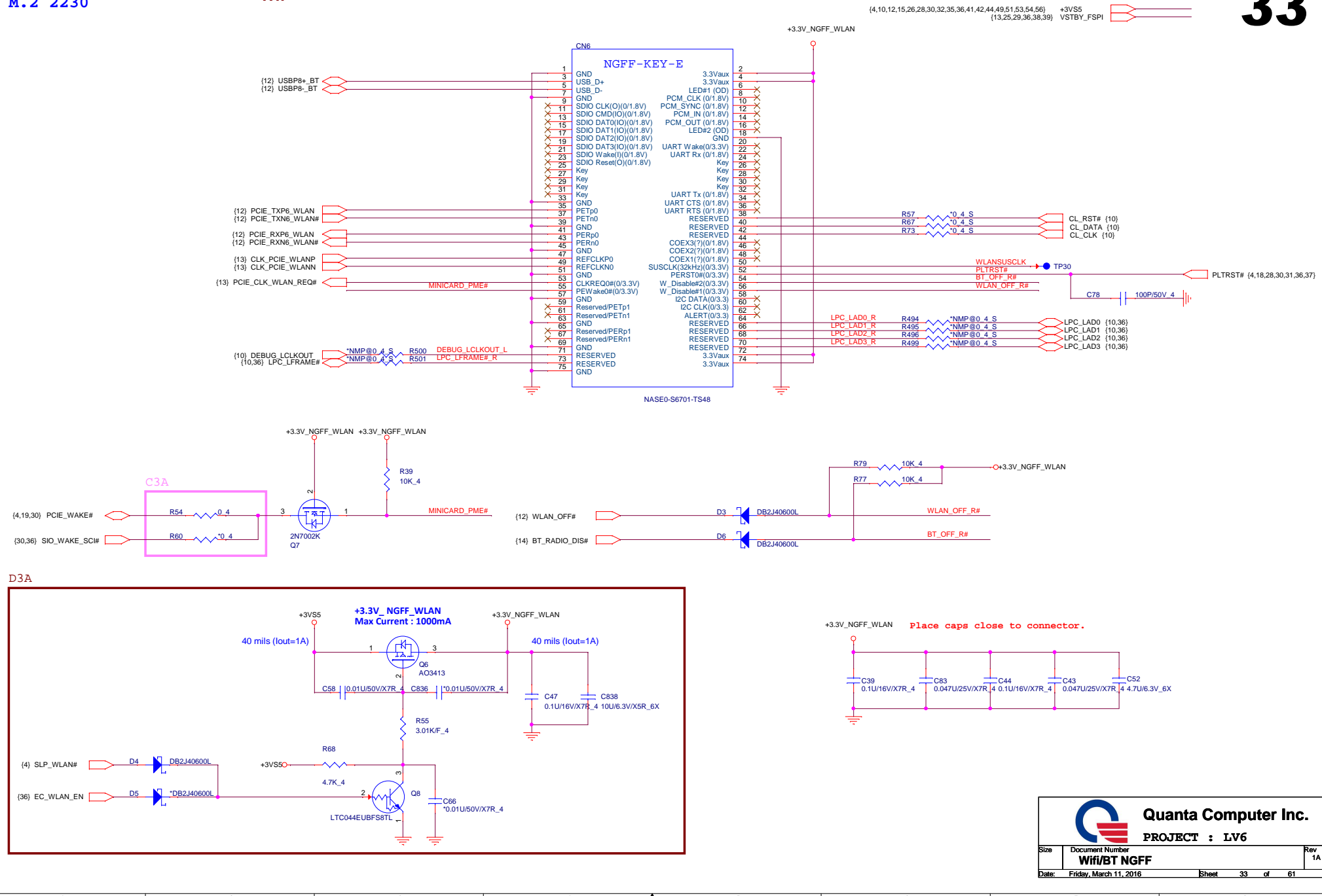
*SSD@10U/6.3V/X5R_6X

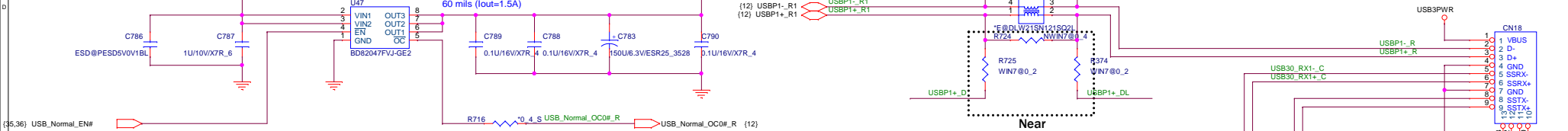


D3A

CR VCC Control







LOW ACTIVE

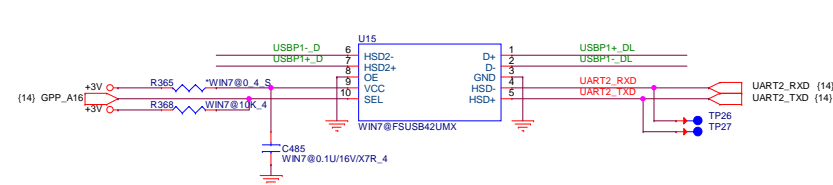
For ESD



For ESD



UART for DEBUG <W7D>



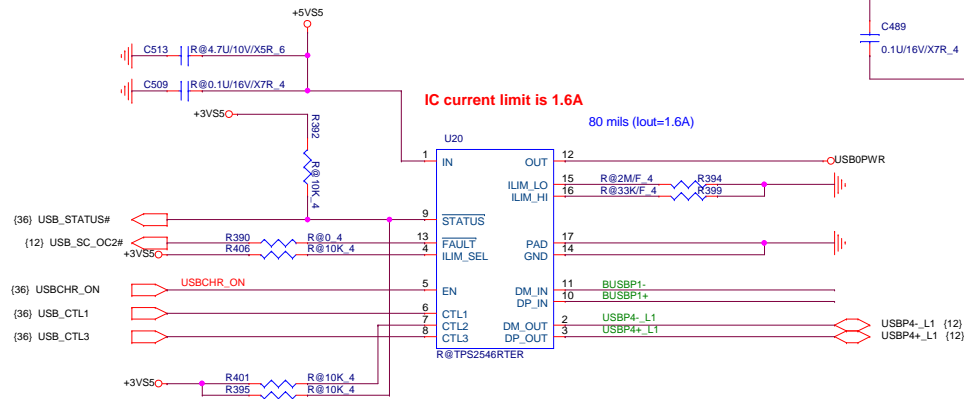
Close to connector

USB3.0 PORT1

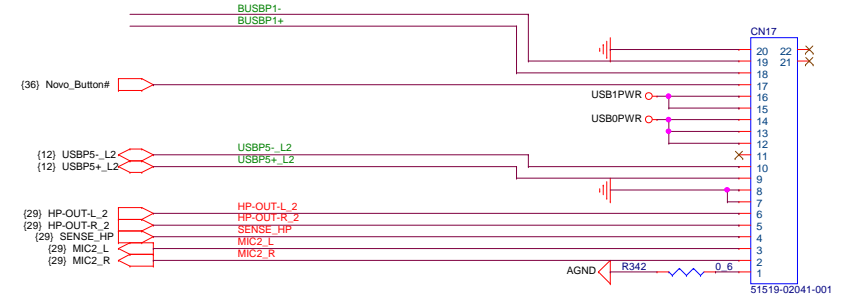
Close to connector

USB Sleep&Charger

<UBC> <UB2>

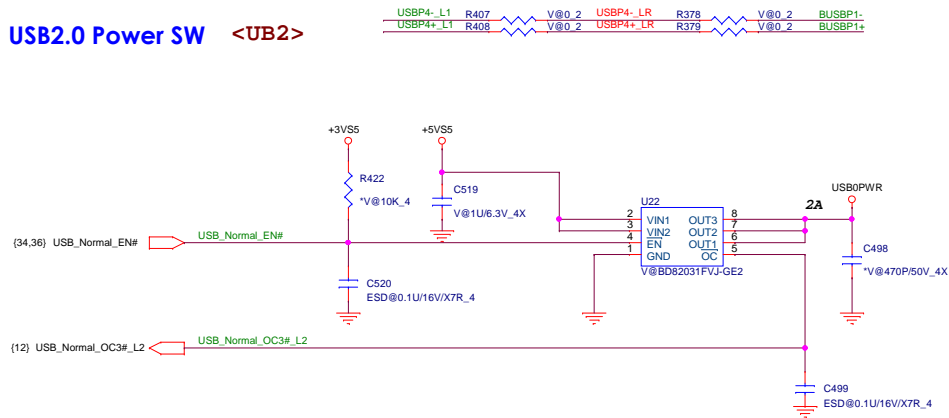


USB3.0 (with AOU5)



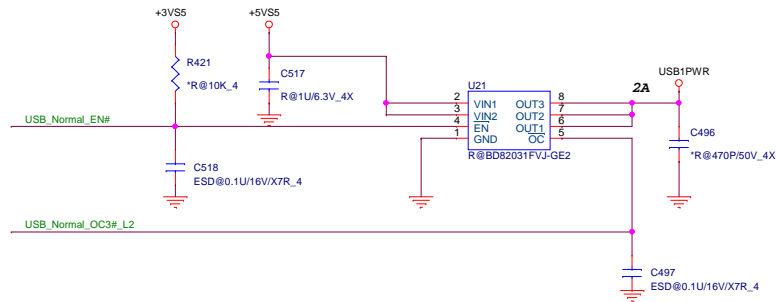
USB2.0 Power SW

<UB2>



USB2.0 Power SW

<UB2>

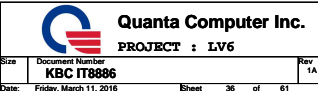


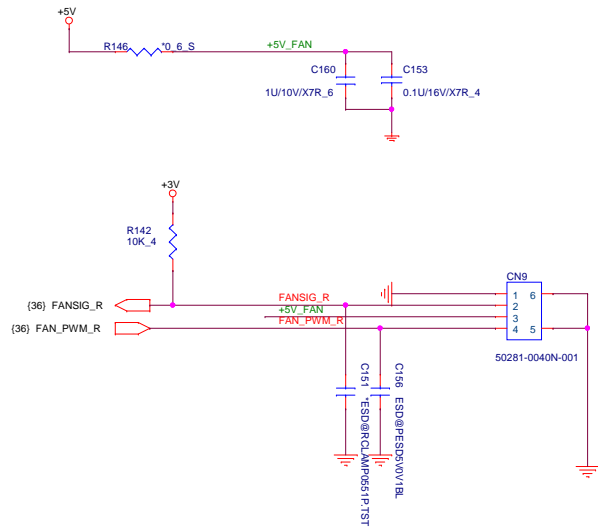
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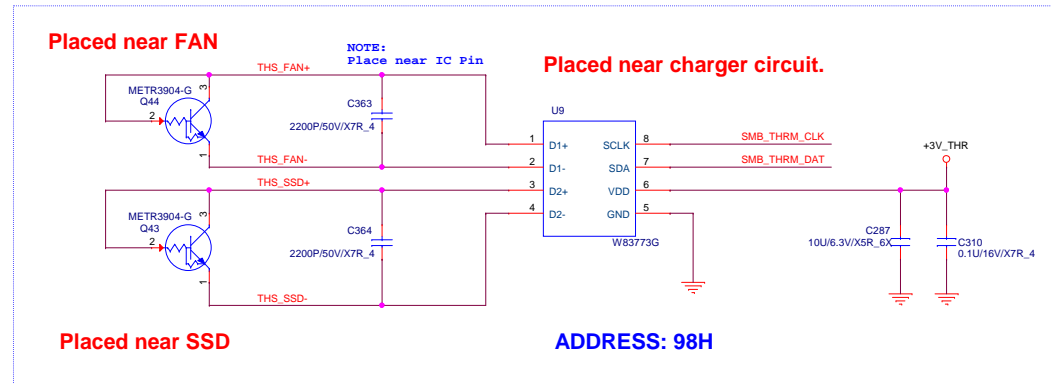
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	S&C/ USB2 (AOU5)	1A

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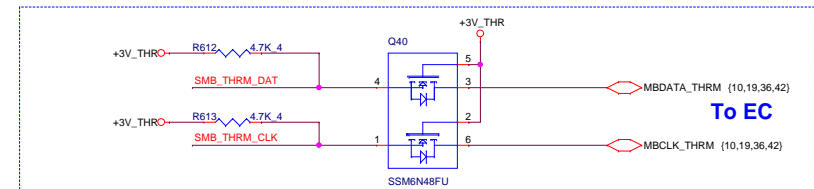
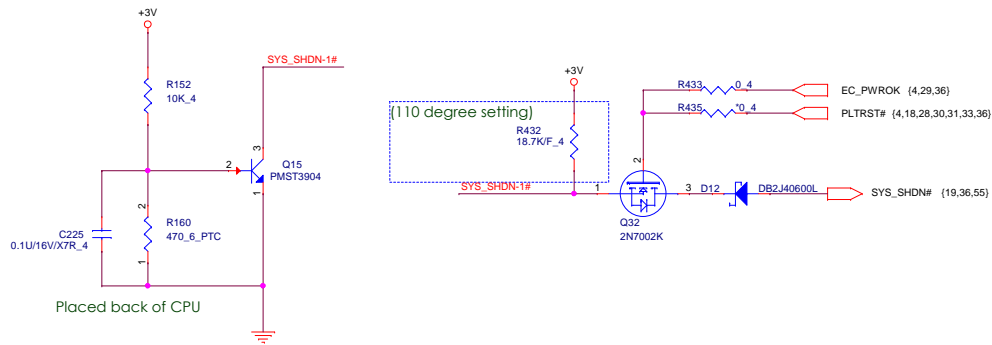




Thermal Sensor

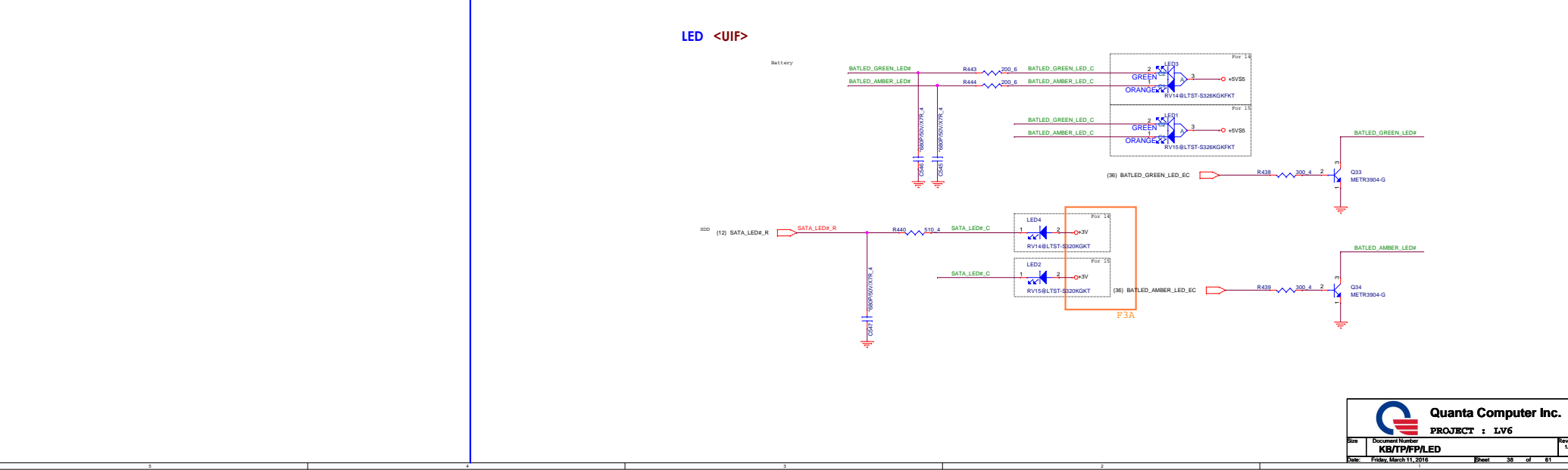
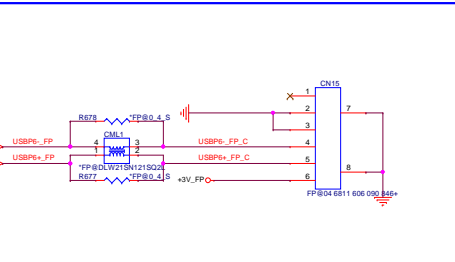
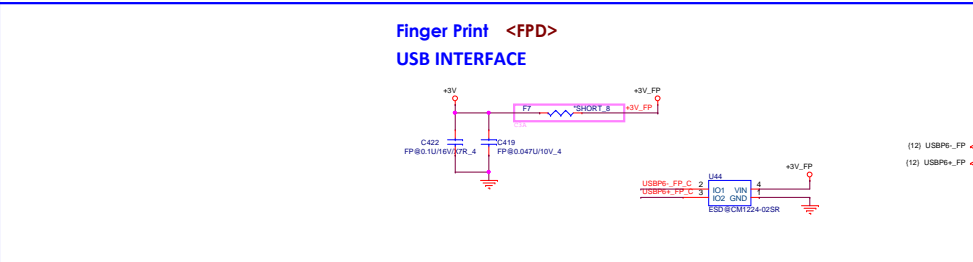
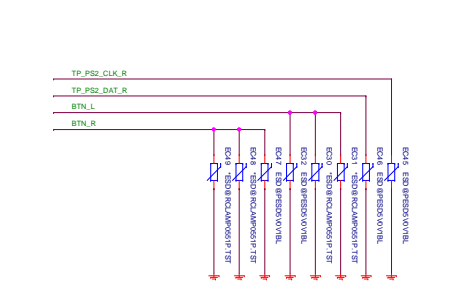
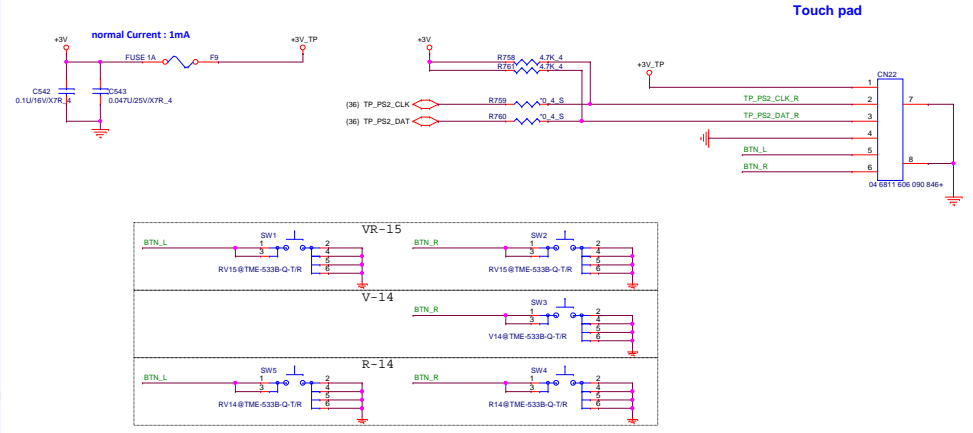
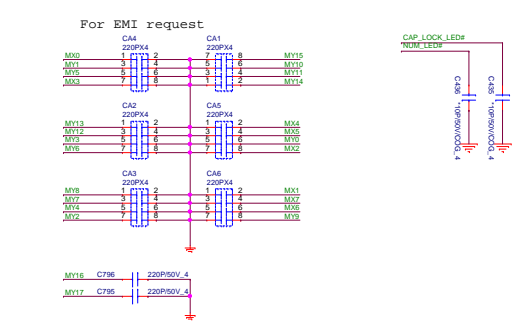
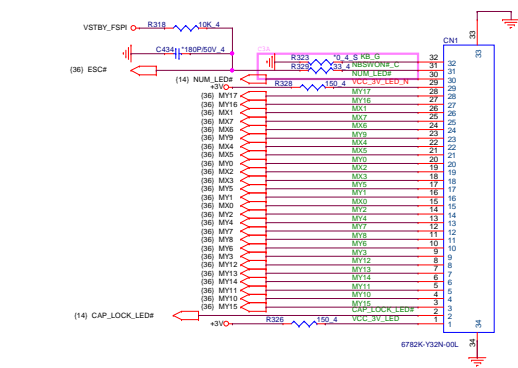


CPU PTC circuit



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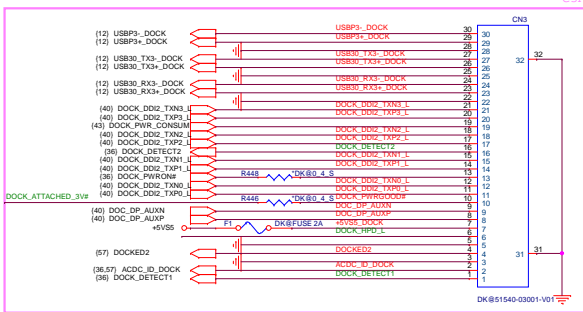


(13,25,29,36,38) VSTBY_FSPI
(26,27,29,31,37,52,53) +5V
(2,4,10,11,12,13,14,15,17,18,25,26,27,29,30,31,34,36,37,38,40,41,42,45,49,52,53,54) +3V
(4,34,35,38,41,42,44,45,48,50,51,53,54,56) +5VSB
(57) DOCK-PWR20-IN

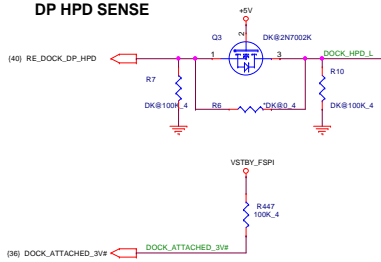


VSTBY_FSPI R469 20K_4 DOCK_DETECT1
VSTBY_FSPI R449 20K_4 DOCK_DETECT2

C3A

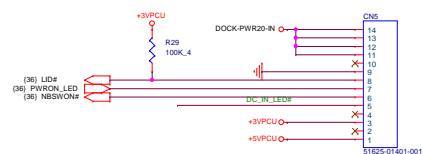


DP HPD SENSE

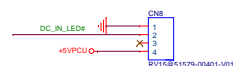
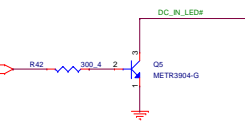


(40) RE_DOCK_DP_HPDI DOCK_HPDI_L

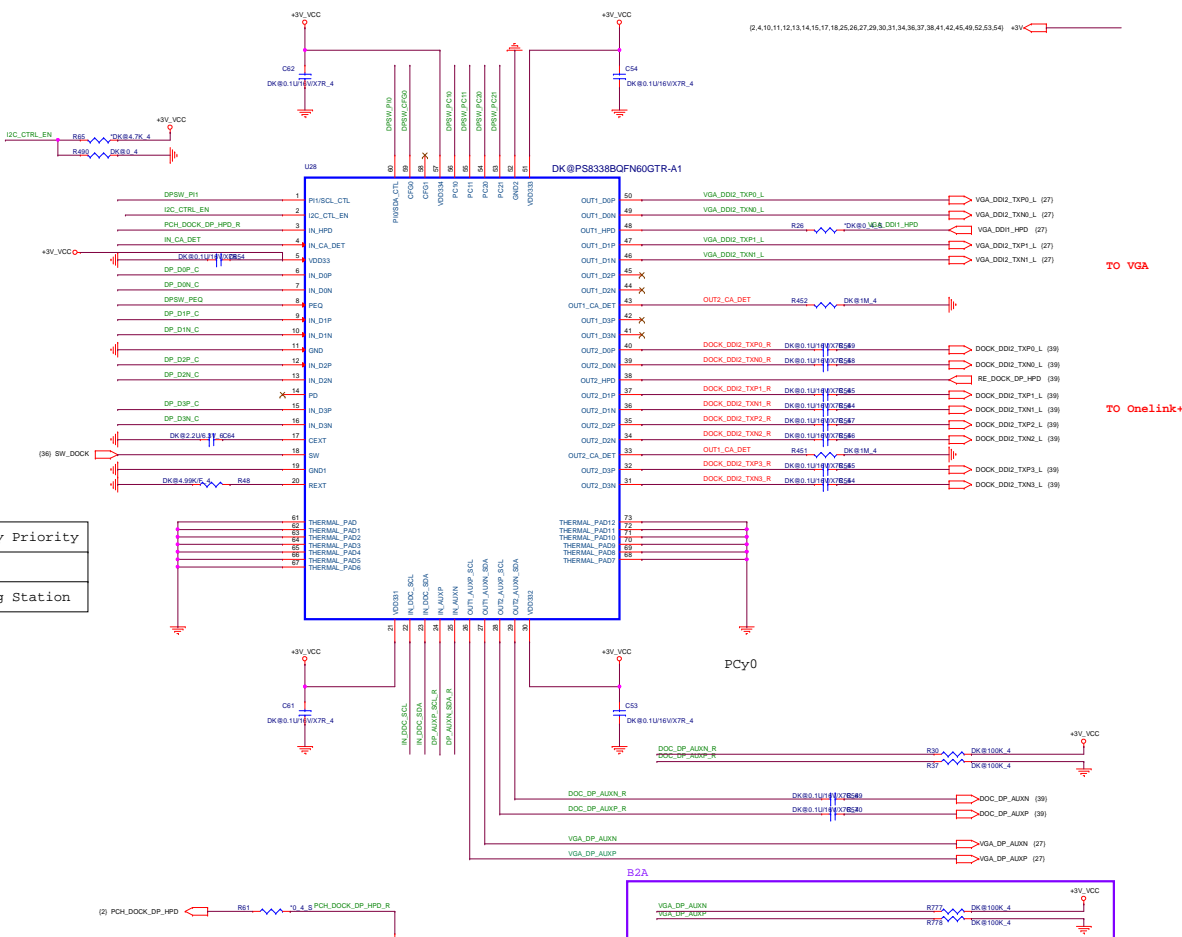
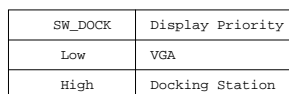
(36) DOCK_ATTACHED_3V# DOCK_ATTACHED_3V#



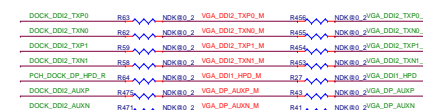
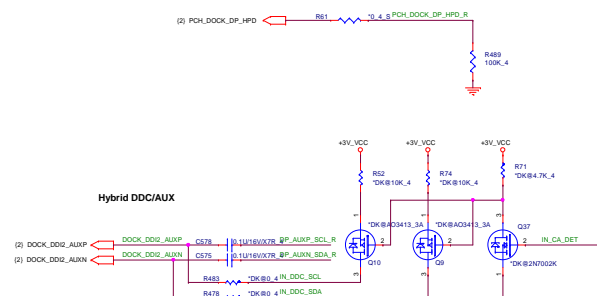
(36) DC_IN_LED_EC

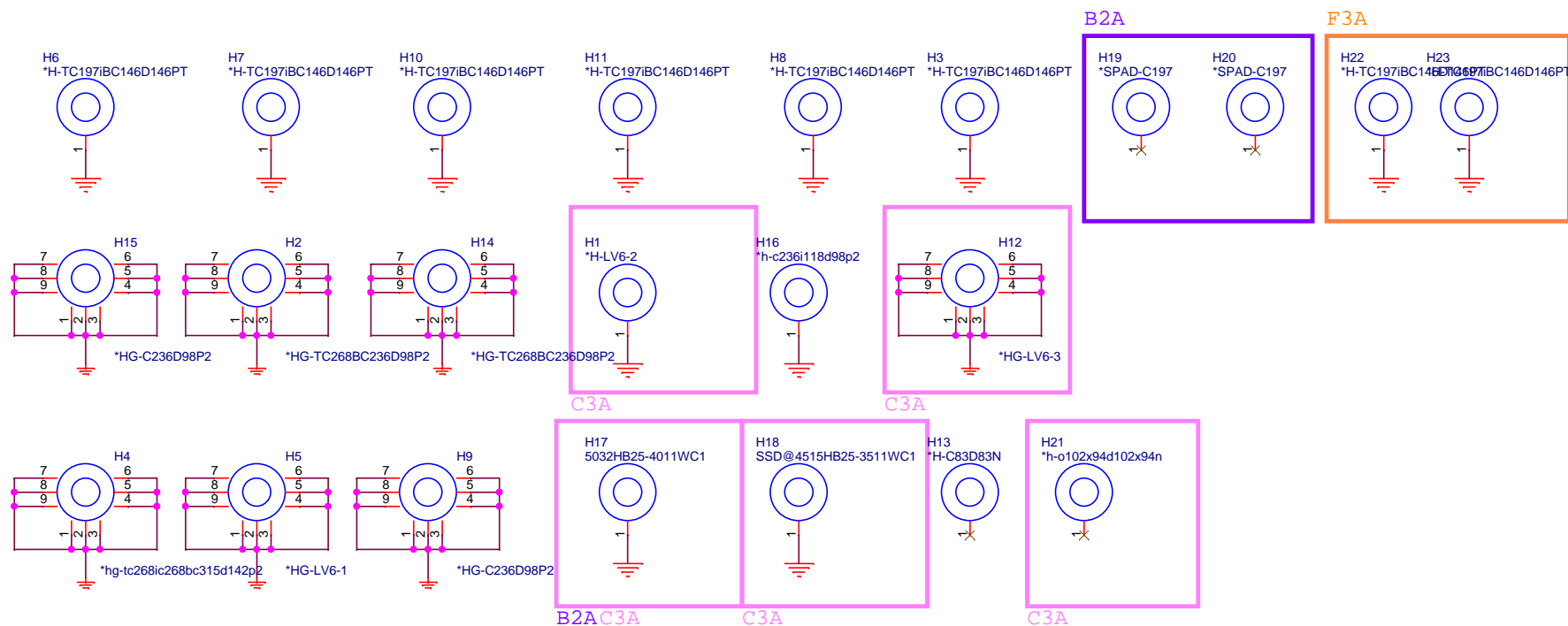


C3A

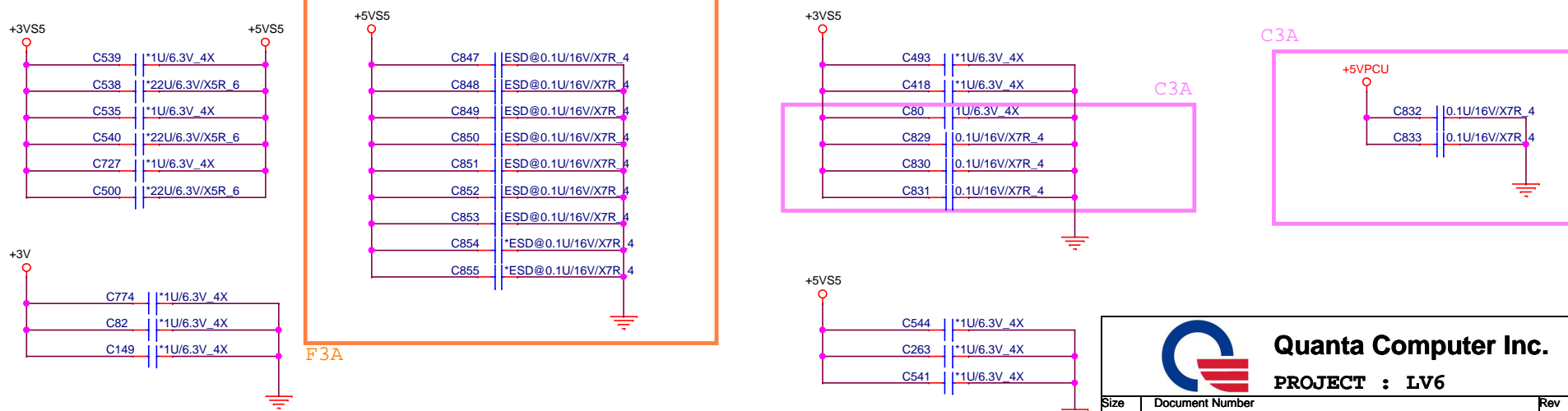


PEQ	L	11.5dB (Default)
	H	14.5dB
	M	8.5dB
PI0	L	Automatic EQ enable (default)
	H	Automatic EQ disable
PI1	L	Auto test disable & input offset cancellation enable(default)
	H	Auto test enable & input offset cancellation enable
CFG0	M	Auto test enable & input offset cancellation enable
	L	Control Switching Mode (Default)
PCY0 (AUX Interception)	L	Automatic Switching Mode
	L	Link training (Default)
	H	800mV/ 0db
PCY1 (Swing)	M	400mV/ 0db
	L	Default
	H	+20%
	M	-16.7%

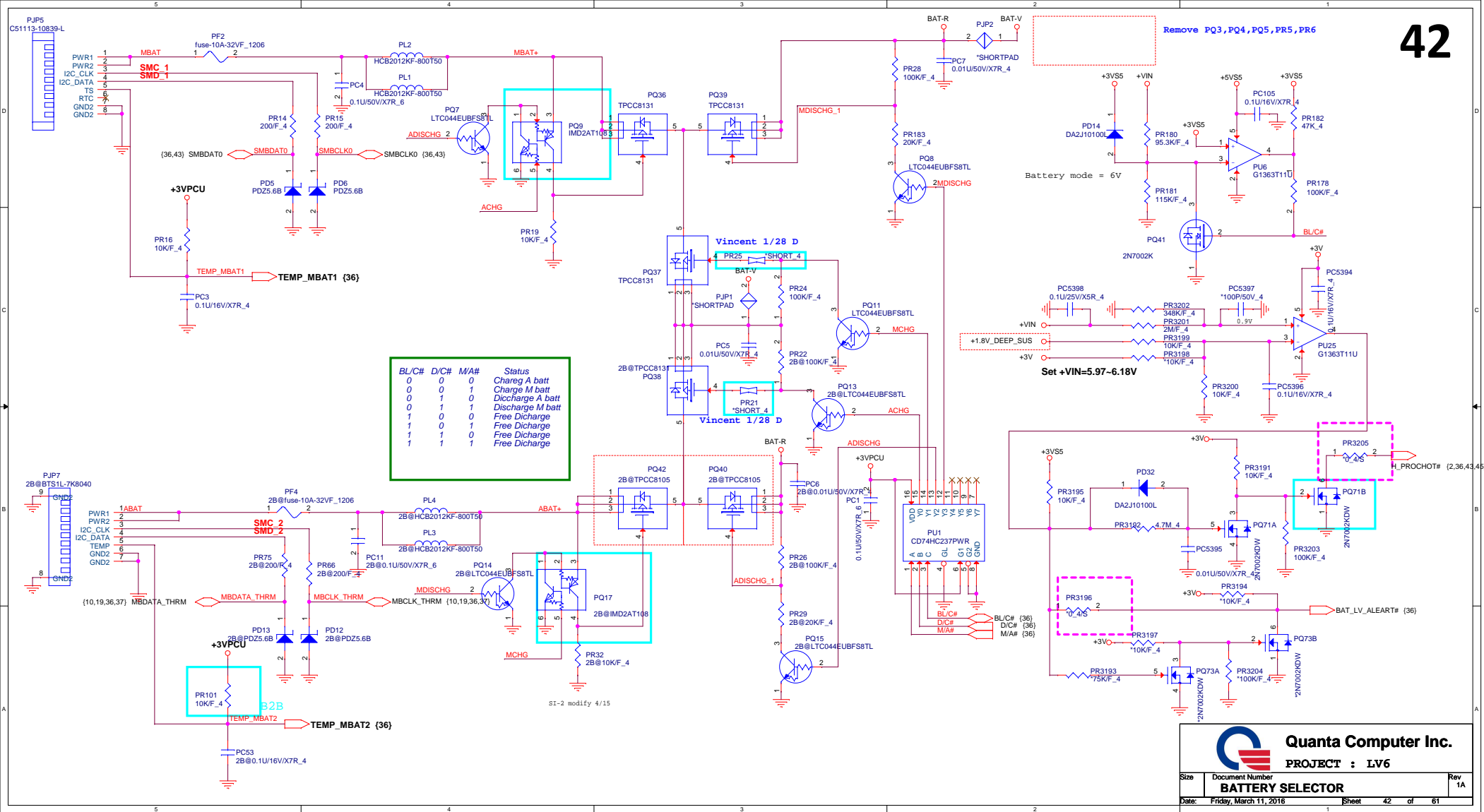


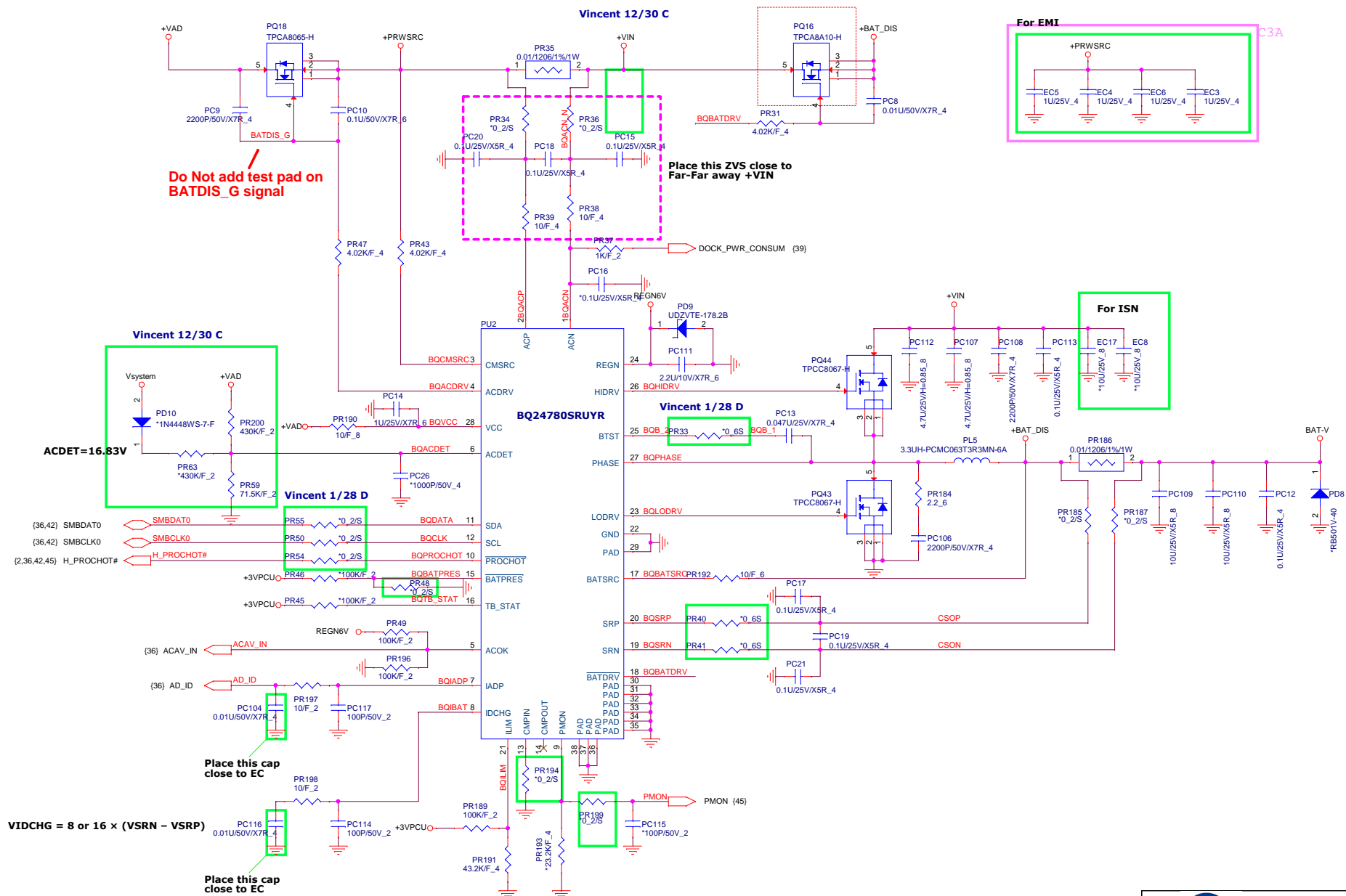


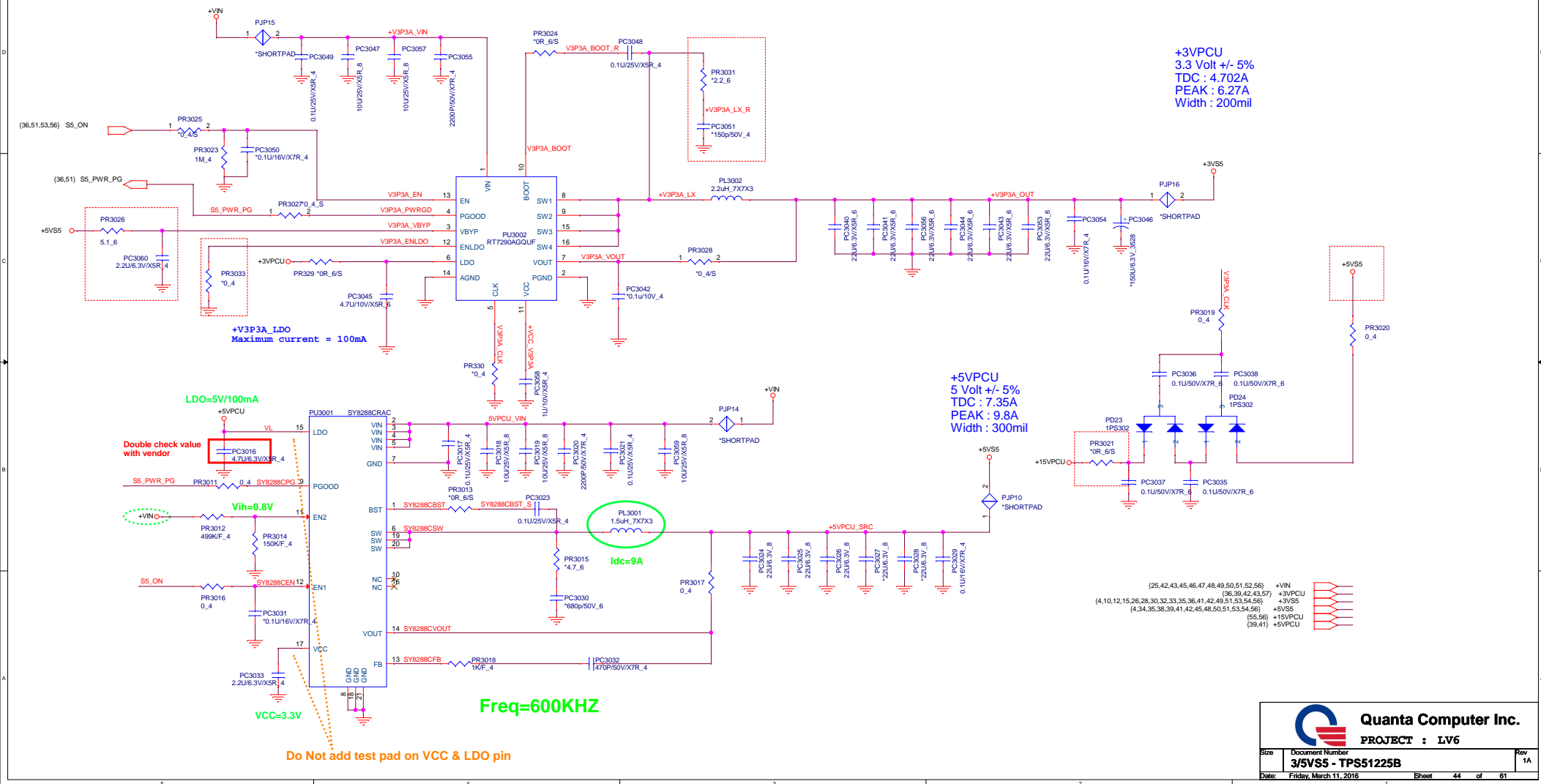
<EMC>

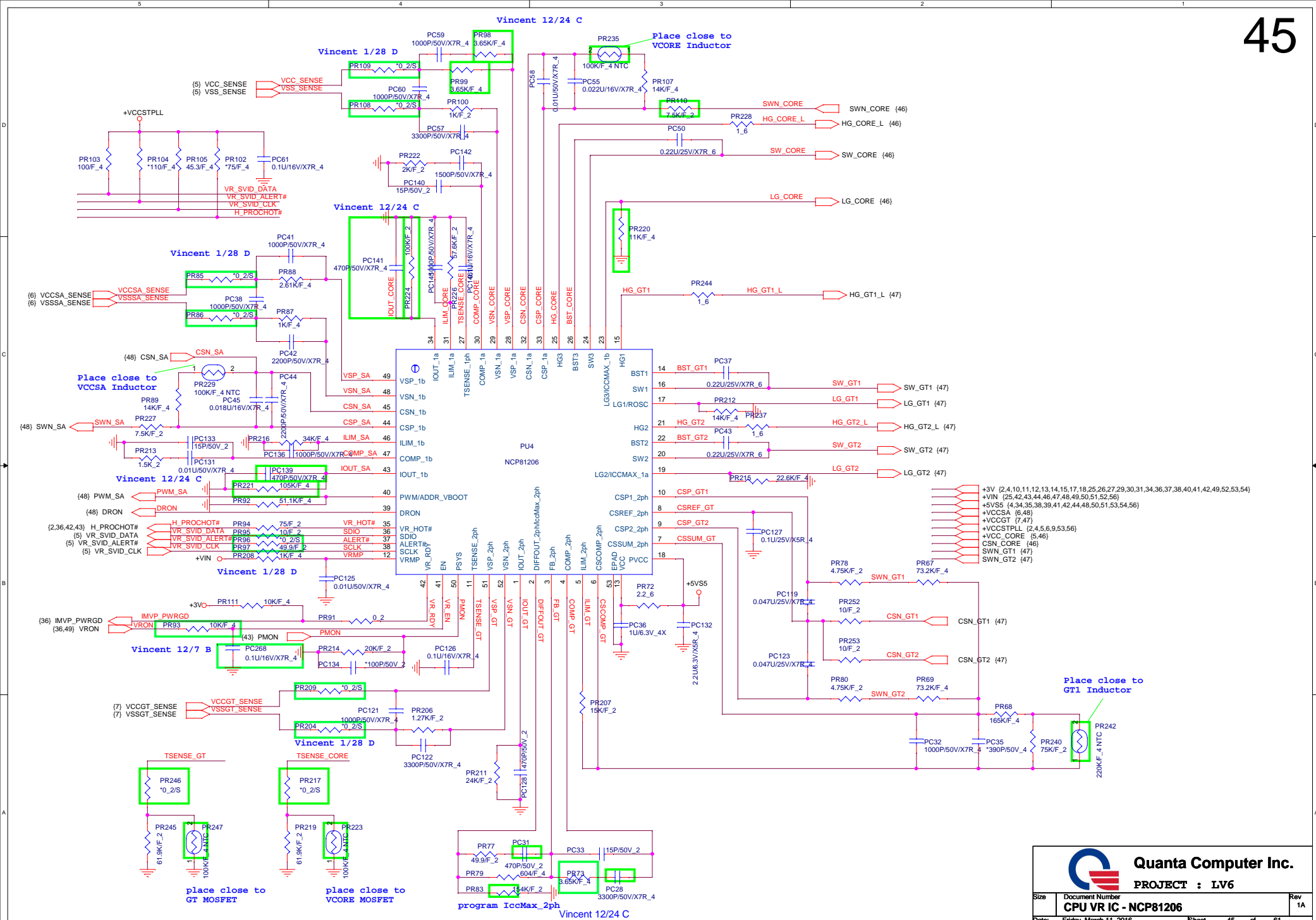


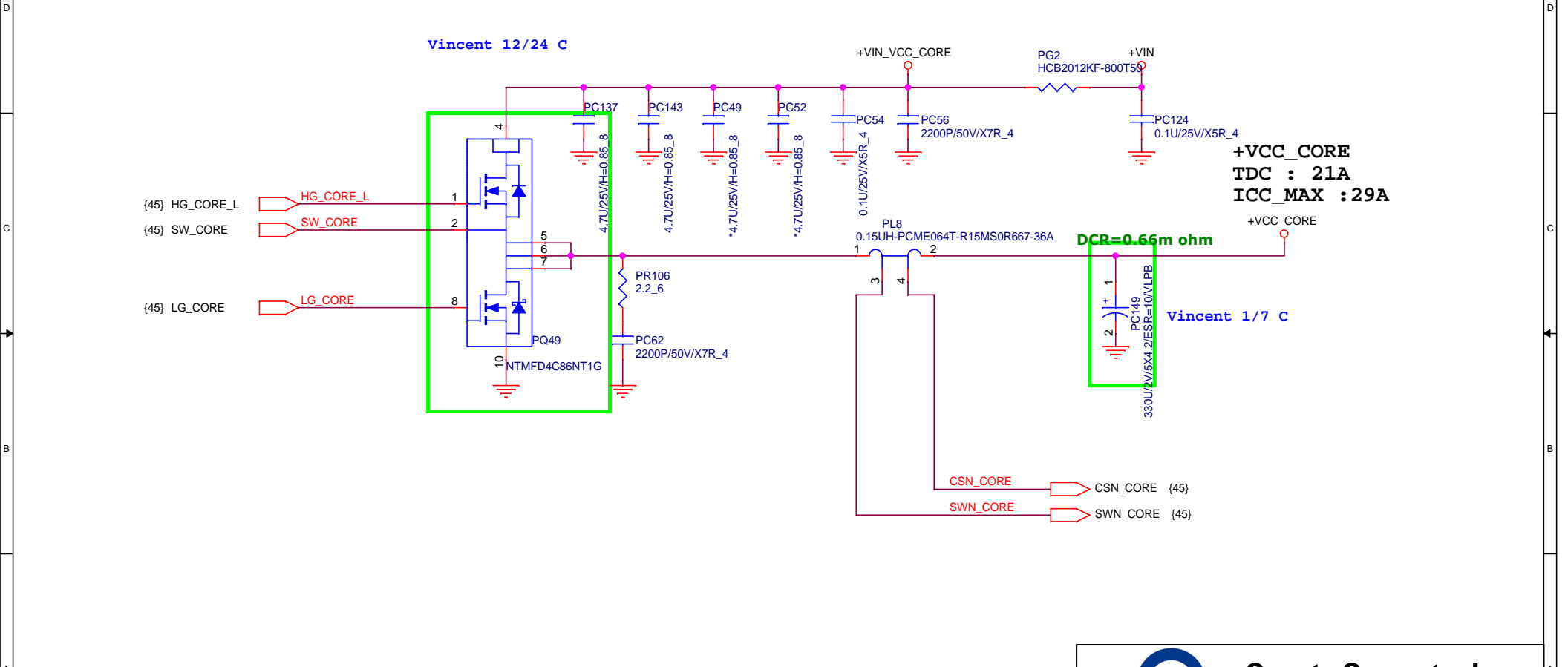
Quanta Computer Inc.
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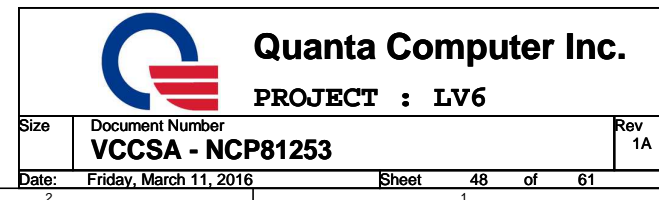


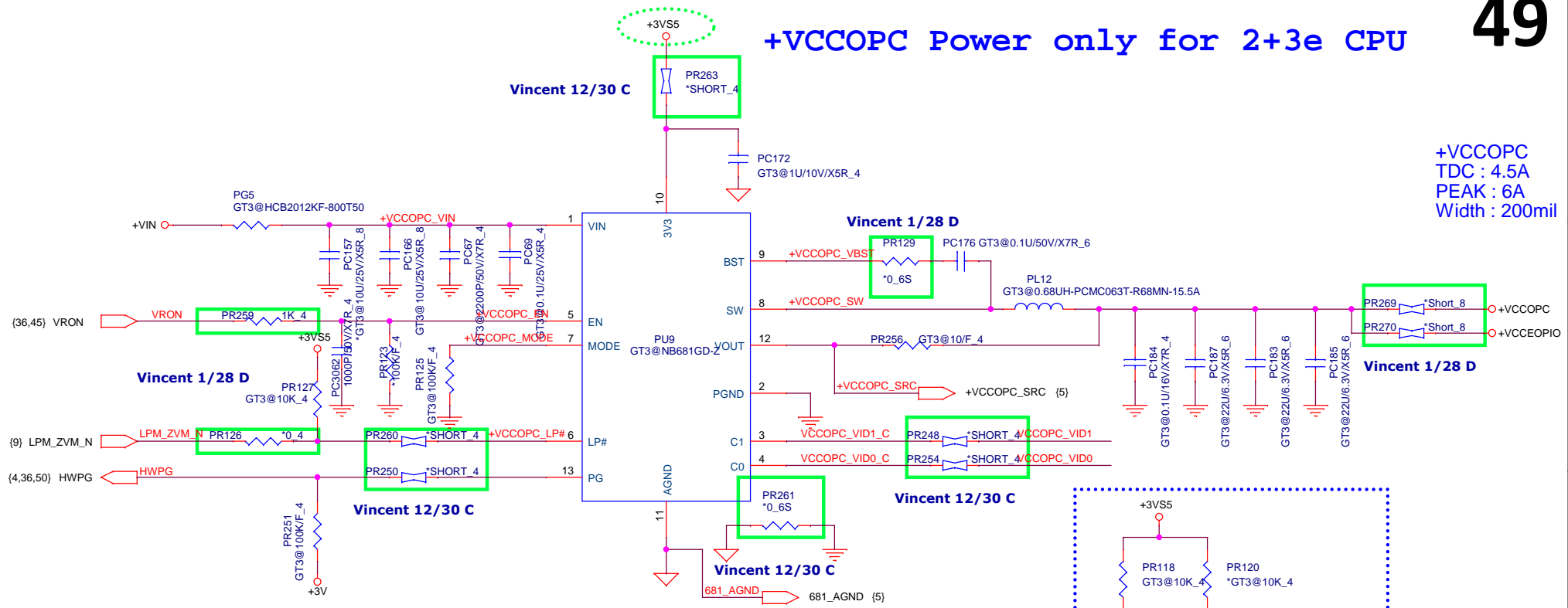






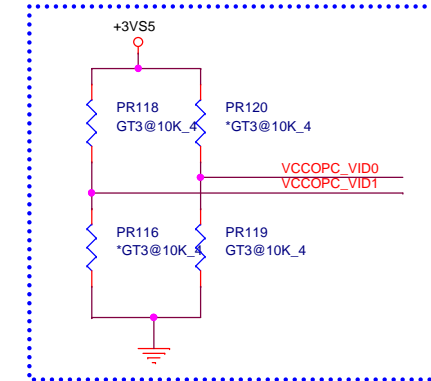
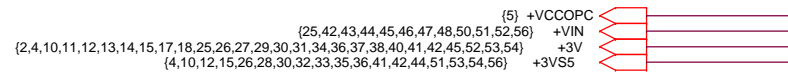
 <div> Quanta Computer Inc. PROJECT : LV6 </div>		
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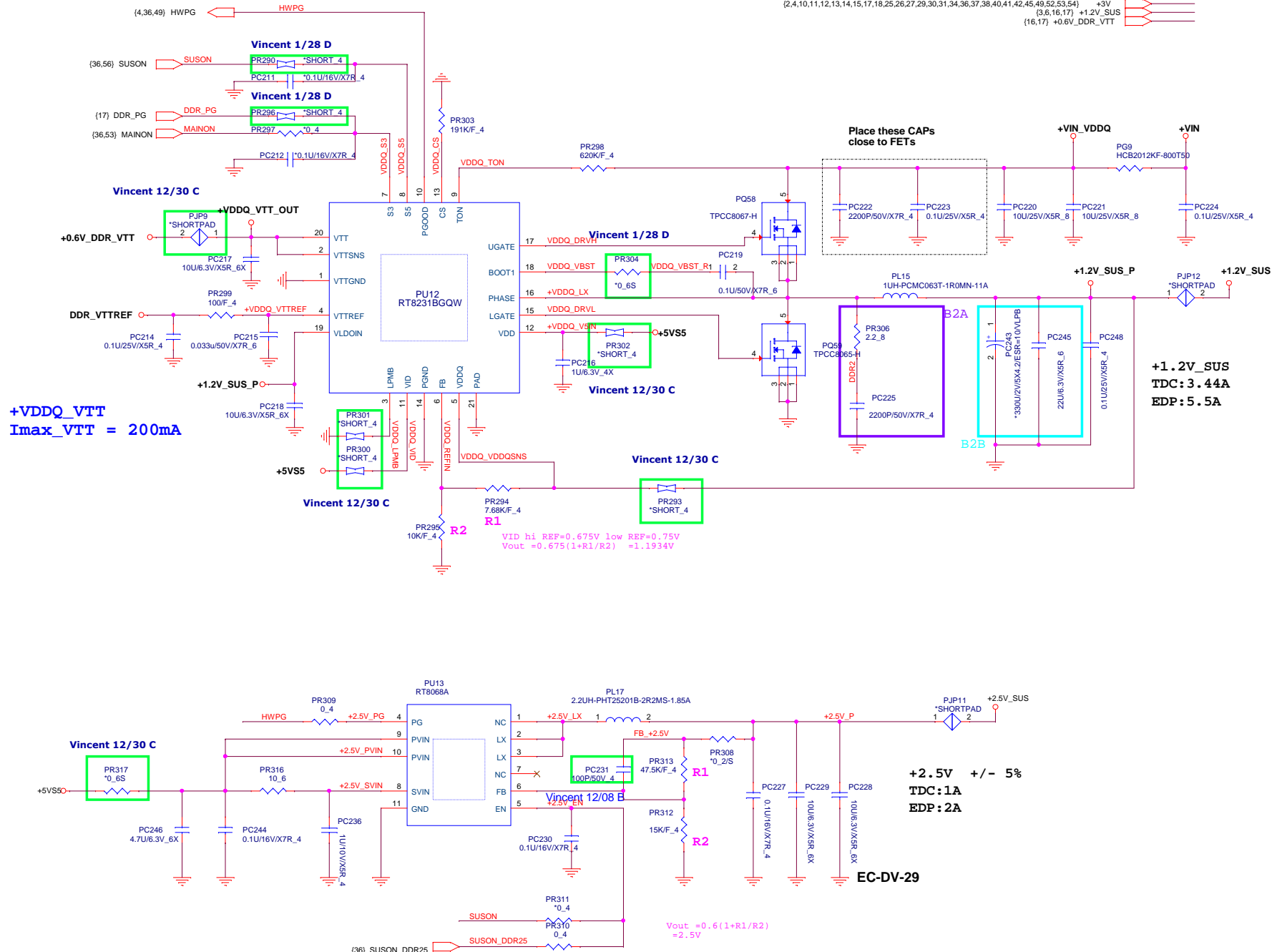


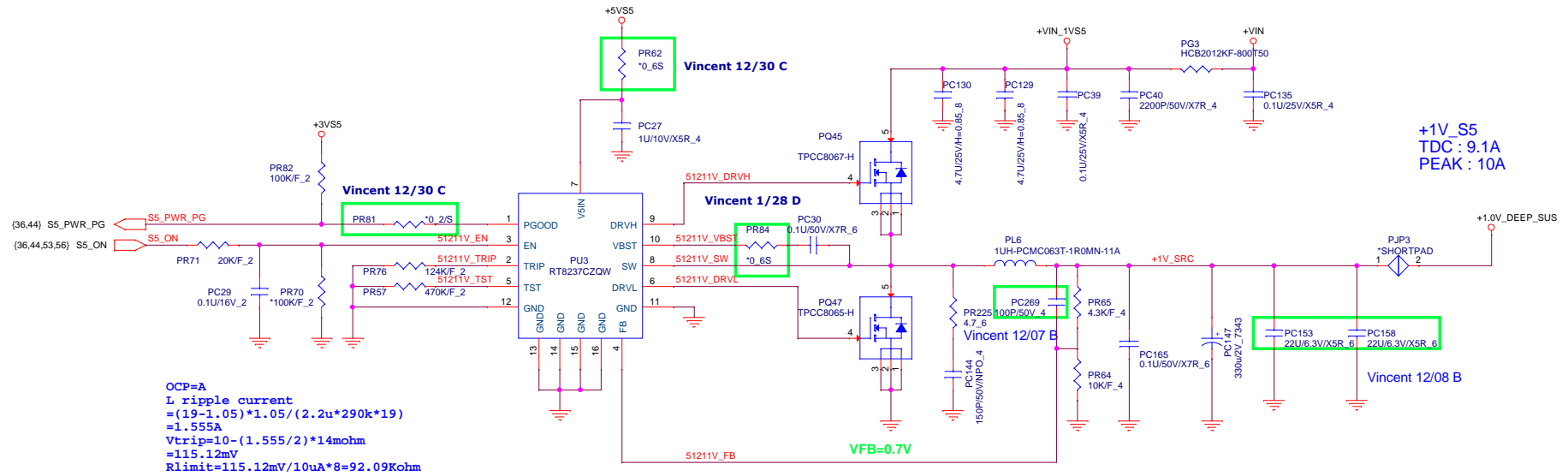
Mode	VR Rail
0 ohm	VCCIO
Floating	PRIMCORE
100K	EDRAM/EOPIC
150K	Other

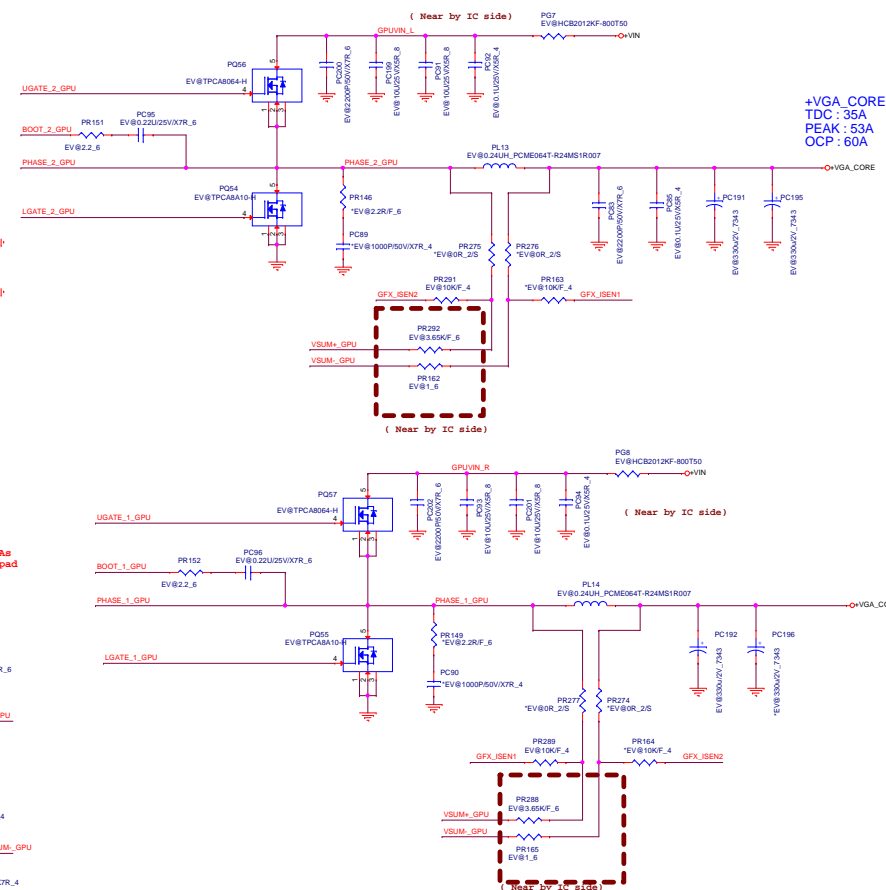
	LP#	C1	C0	Vo
VCCEDRAM	0	X	X	0V
	1	0	0	0.8V(MSM)
	1	0	1	0.95V
	1	1	0	1.0V
	1	1	1	1.05V

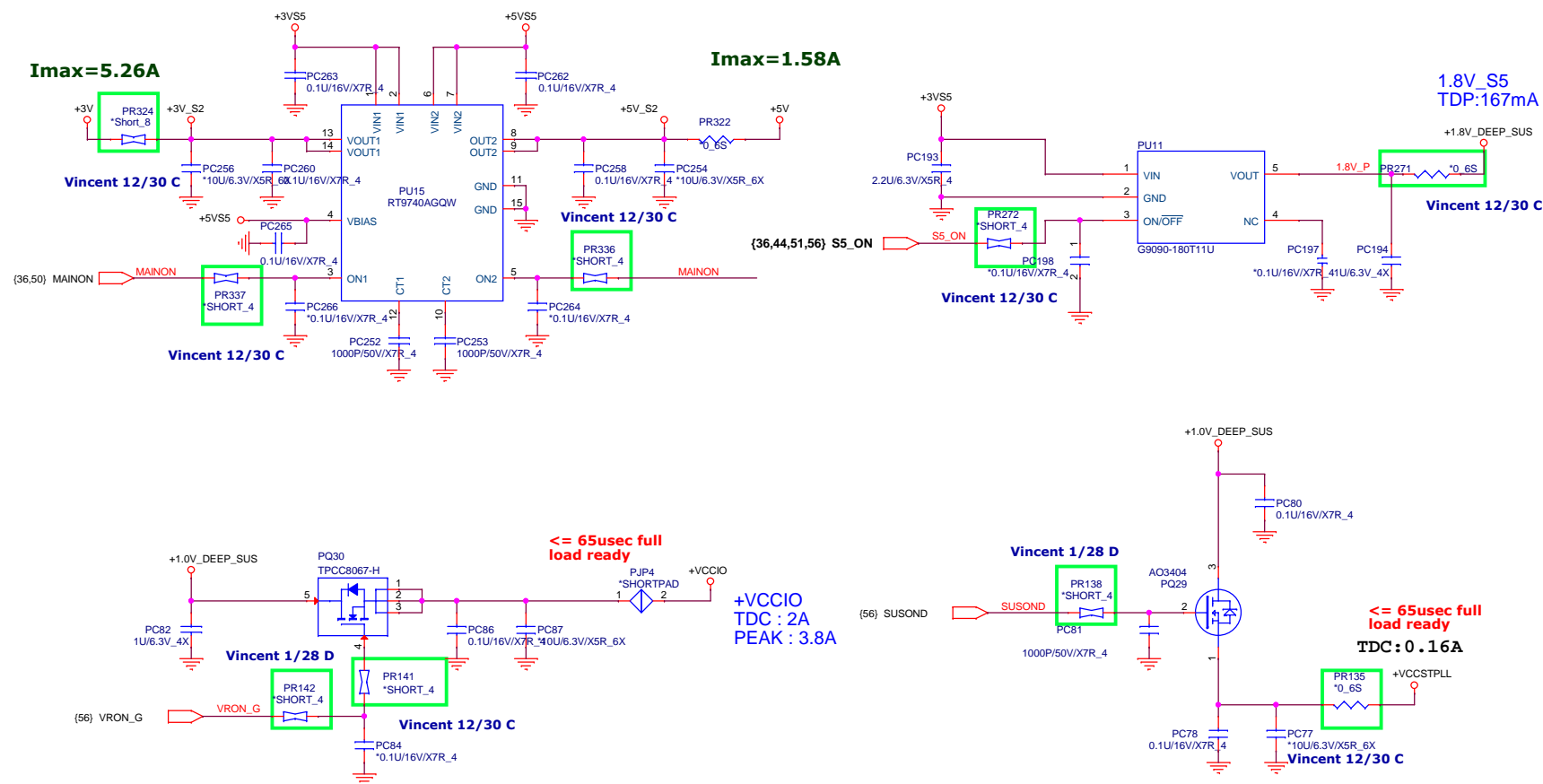


{25,42,43,44,45,46,47,48,49,51,52,56} +VIN
 {4,34,35,38,39,41,42,44,45,48,51,53,54,56} +5VS5
 {2,4,10,11,12,13,14,15,17,18,25,26,27,29,30,31,34,36,37,38,40,41,42,45,49,52,53,54} +3V
 {3,6,16,17} +1.2V_SUS
 {16,17} +0.6V_DDR_VTT

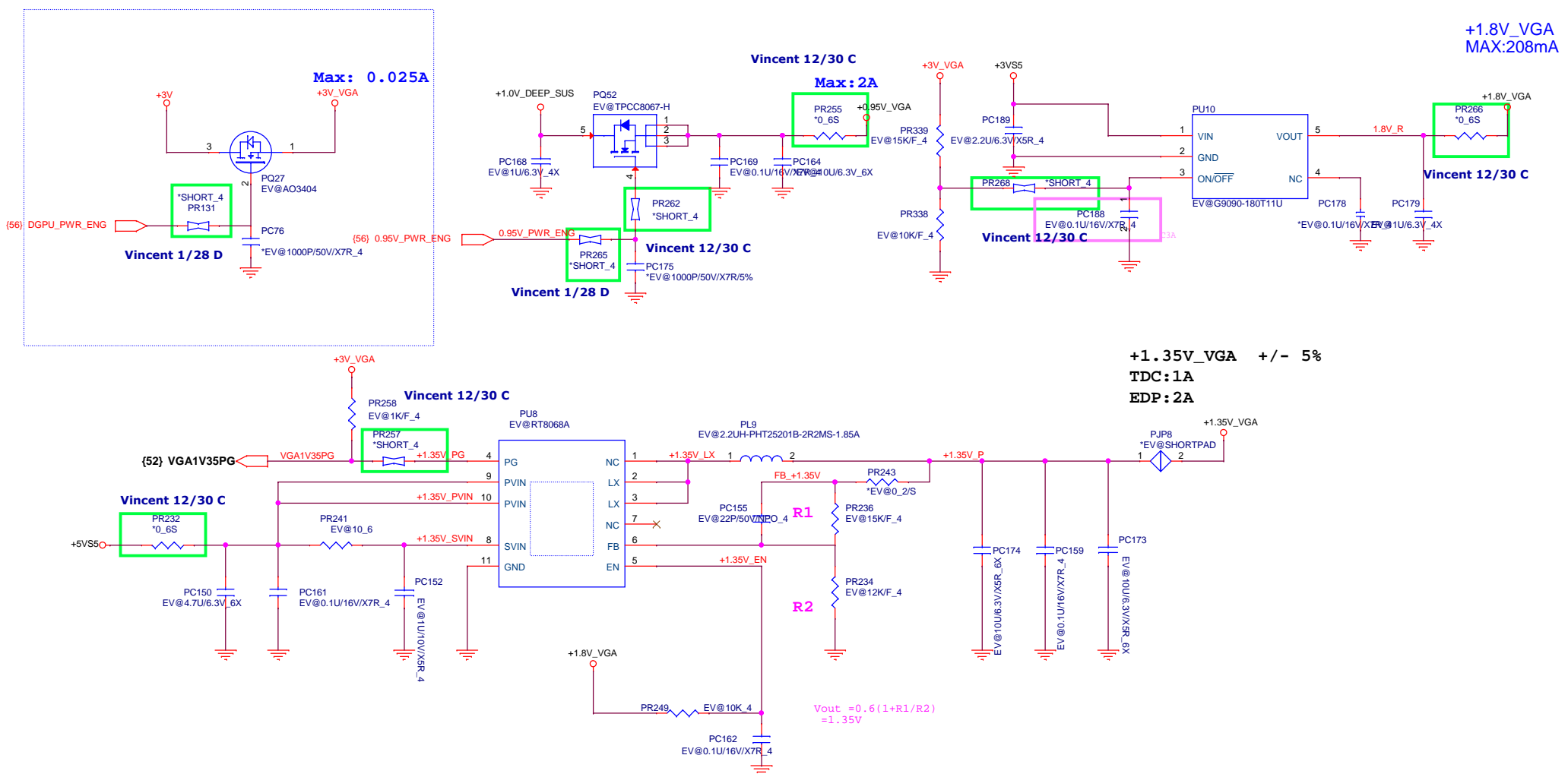








+1.8V_VGA(G9090-180T11U)
+1.35V_VGA(RT8068A)

+1.8V_VGA
MAX:208mA

+1.35V_VGA +/- 5%
TDC:1A
EDP:2A

$$V_{out} = 0.6(1 + R_1/R_2) = 1.35V$$



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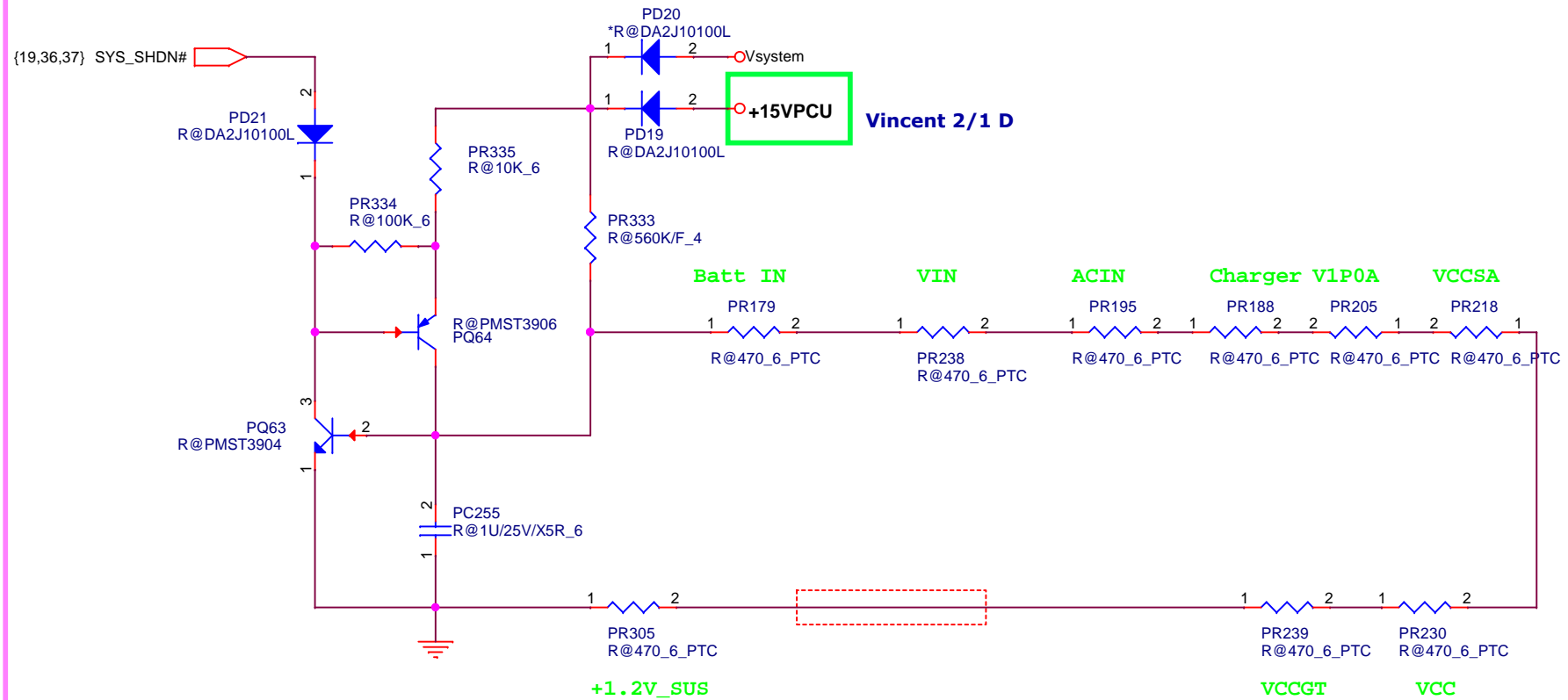
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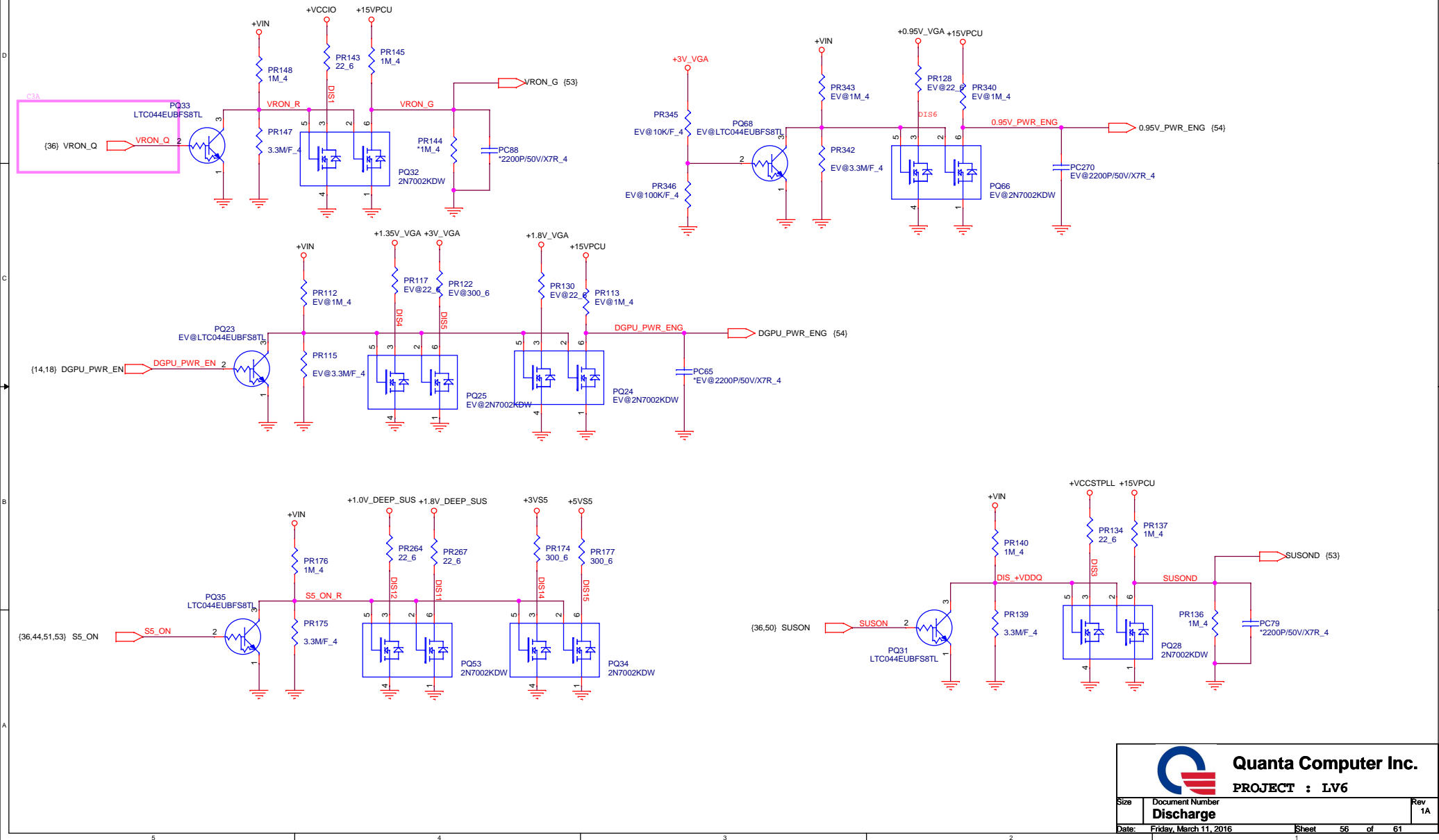
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1A



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	PTC Circuit	1A
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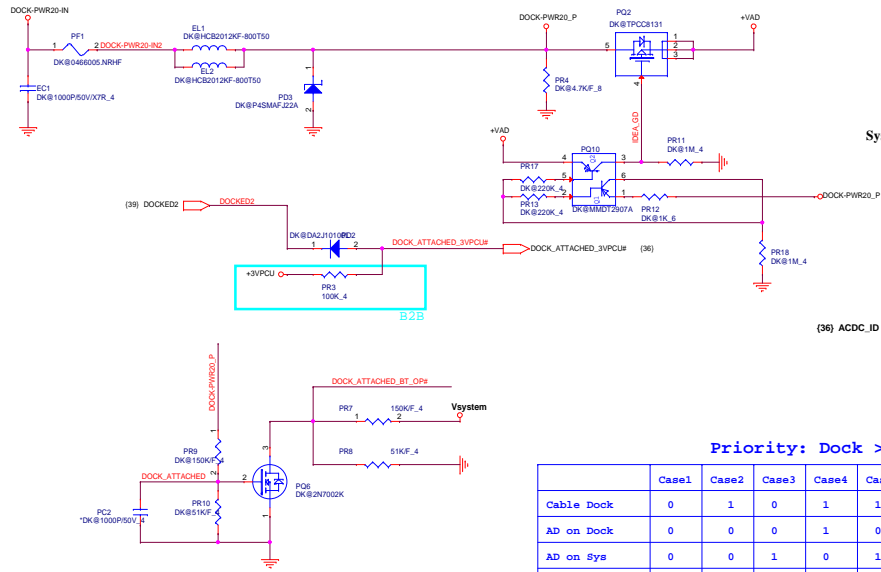


Quanta Computer Inc.

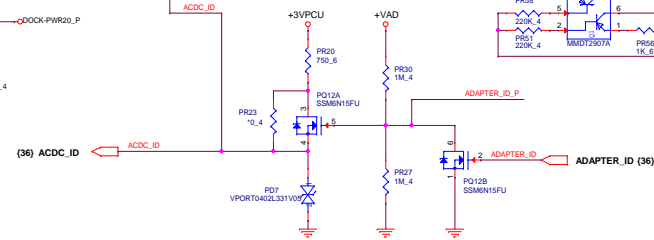
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	Discharge	1A
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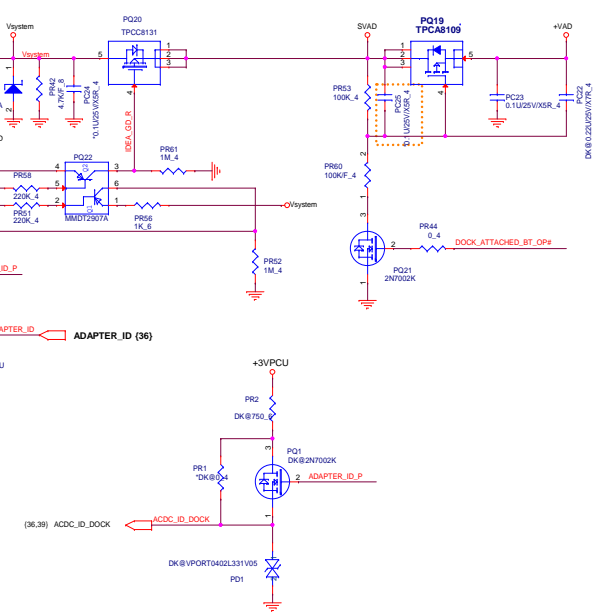
For Dock



System Adaptor

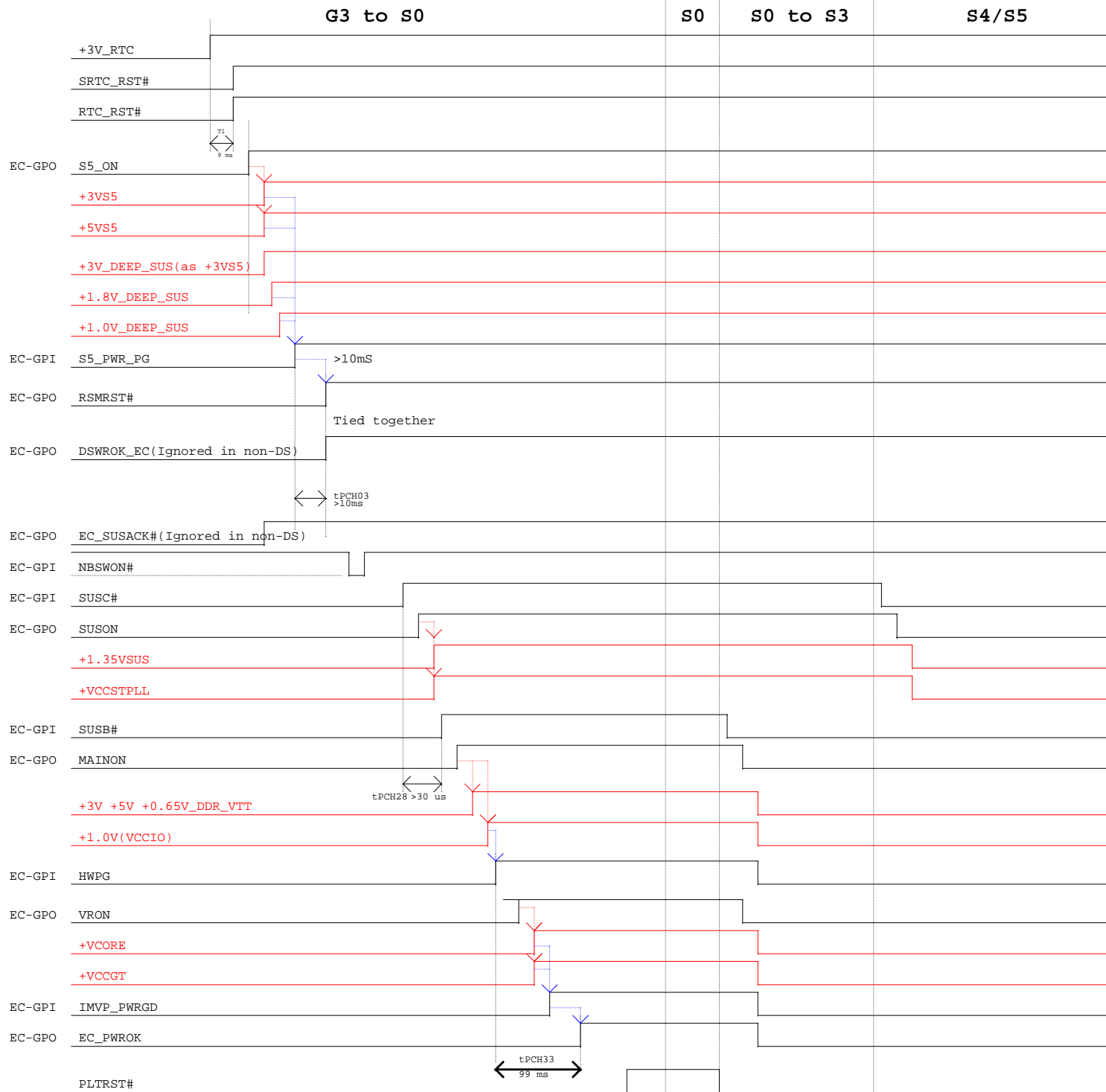


For System



Priority: Dock > DC_IN


	Case1	Case2	Case3	Case4	Case5	Case6	Case7	Case8	Case9	Case10
Cable Dock	0	1	0	1	1	0	1	1	0	1
AD on Dock	0	0	0	1	0	0	1	1	0	1
AD on Sys	0	0	1	0	1	1	1	0	1	1
Power Source	Batt	Batt	AD on Sys	AD on Dock	AD on Sys	AD on Sys	AD on Dock	AD on Dock	AD on Sys	AD on Dock



2015	EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
	B2A	2	12/7	R780	Reserve PU 10K for
		4	12/7	R763	Add PU Res 10K for LAN_WAKE#.
		4	12/7	R764	Add PU Res 10K for VRALERT#.
		5	12/7	C819	Add Cap 1U for VCCSTG_G20.
		14	12/7	R768, R767	Add Board ID for SKYLAKE/ KBYLAKE.
		26	12/7	R769 、 R770 、 R771 、 R772 、 R773 、 R774 、 R775 、 R776	Add ohm for HDMI test
		30	12/7	CN14	Modify LAN connect pin define for LED
		31	12/7	CN19	Remove GND of stand pin for HDD connect
		31	12/7	CN12	Modify ODD connect to match FFC pin define
	B2B (R310)	30	12/18	CN14	Modify LAN connect pin define for LED
		4, 36	12/18	D10 、 R779 、 R780	Reserve DNBSWON# PU to +3VS5 and short 0 ohm
		13, 30	12/25	C755 、 C763 、 C359 、 C360	RTC CAP tuning
		29	12/25	R21 、 R16 、 R3 、 R8	FOR EMI

SIT-STAGE

[illegible]

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